Boost/SEPIC/Inverting DC/DC Converter with 1A, 65V Switch, Soft-Start and Synchronization

FEATURES

- **1A, 65V Power Switch**
- **Adjustable Switching Frequency**
- **Single Feedback Resistor Sets V_{OUT}**
- **Synchronizable to External Clock**
- High Gain $\overline{SHDN}$ Pin Accepts Slowly Varying Input Signals
- Wide Input Voltage Range: 2.55V to 40V
- Low V_{CESAT} Switch: 400mV at 0.75A (Typical)
- Integrated Soft-Start Function
- Easily Configurable as a Boost, SEPIC, or Inverting Converter
- User Configurable Undervoltage Lockout (UVLO)
- Pin Compatible with LT3580
- Tiny Thermally Enhanced 8-Lead 3mm × 3mm DFN and 8-Lead MSOP Packages
- AEC-Q100 Qualification in Progress

APPLICATIONS

- VFD Bias Supplies
- TFT-LCD Bias Supplies
- GPS Receivers
- DSL Modems
- Local Power Supply

DESCRIPTION

The LT®8580 is a PWM DC/DC converter containing an internal 1A, 65V switch. The LT8580 can be configured as either a boost, SEPIC or inverting converter.

The LT8580 has an adjustable oscillator, set by a resistor from the RT pin to ground. Additionally, the LT8580 can be synchronized to an external clock. The switching frequency of the part may be free running or synchronized, and can be set between 200kHz and 1.5MHz.

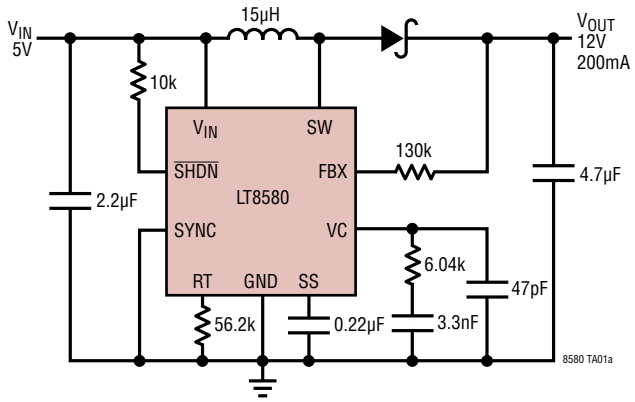
The LT8580 also features innovative $\overline{SHDN}$ pin circuitry that allows for slowly varying input signals and an adjustable undervoltage lockout function.

Additional features such as frequency foldback and soft-start are integrated. The LT8580 is available in tiny thermally enhanced 3mm × 3mm 8-lead DFN and 8-lead MSOP packages.

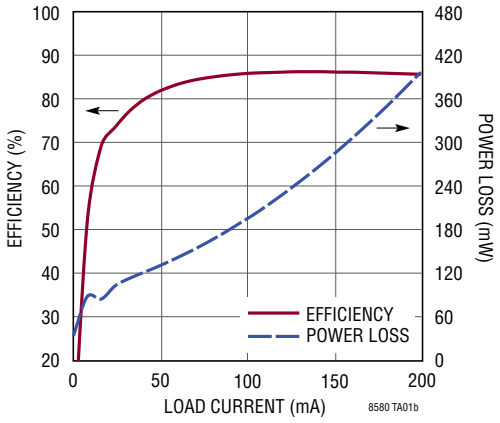
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TYPICAL APPLICATION

1.5MHz, 5V to 12V Boost Converter



Efficiency and Power Loss

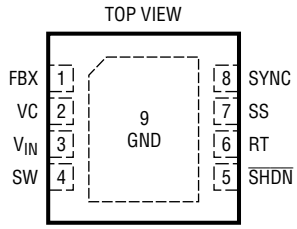


Rev. B

ABSOLUTE MAXIMUM RATINGS (Note 1)

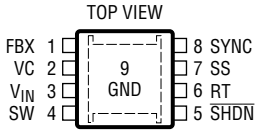
V_{IN} Voltage ..... –0.3V to 40V
SW Voltage ..... –0.4V to 65V
RT Voltage ..... –0.3V to 5V
SS Voltage ..... –0.3V to 2.5V
FBX Voltage 5V
FBX Current ..... –1mA
VC Voltage ..... –0.3V to 2V
$\overline{SHDN}$ Voltage ..... –0.3V to 40V
SYNC Voltage ..... –0.3V to 5.5V
Operating Junction Temperature Range
LT8580E (Notes 2, 5) ..... –40°C to 125°C
LT8580I (Notes 2, 5) ..... –40°C to 125°C
LT8580H (Notes 2, 5) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



MS8E PACKAGE
8-LEAD PLASTIC MSOP

θ_{JA} = 35°C/W TO 40°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8580EDD#PBF	LT8580EDD#TRPBF	LGKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT8580IDD#PBF	LT8580IDD#TRPBF	LGKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT8580HDD#PBF	LT8580HDD#TRPBF	LGKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 150°C
LT8580EMS8E#PBF	LT8580EMS8E#TRPBF	LTGKJ	8-Lead Plastic MSOP	–40°C to 125°C
LT8580IMS8E#PBF	LT8580IMS8E#TRPBF	LTGKJ	8-Lead Plastic MSOP	–40°C to 125°C
LT8580HMS8E#PBF	LT8580HMS8E#TRPBF	LTGKJ	8-Lead Plastic MSOP	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8580EMS8E#WPBF	LT8580EMS8E#WTRPBF	LTGKJ	8-Lead Plastic MSOP	–40°C to 125°C
LT8580IMS8E#WPBF	LT8580IMS8E#WTRPBF	LTGKJ	8-Lead Plastic MSOP	–40°C to 125°C
LT8580HMS8E#WPBF	LT8580HMS8E#WTRPBF	LTGKJ	8-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	LT8580E, LT8580I LT8580H	● ●	2.55 2.9		40 40	V V
Positive Feedback Voltage		●	1.185	1.204	1.220	V
Negative Feedback Voltage		●	–3	3	12	mV
Positive FBX Pin Bias Current	V_{FBX} = Positive Feedback Voltage, Current Into Pin	●	81	83.3	85	µA
Negative FBX Pin Bias Current	V_{FBX} = Negative Feedback Voltage, Current Out of Pin	●	81	83.3	86	µA
Error Amplifier Transconductance				200		µmhos
Error Amplifier Voltage Gain				60		V/V
Quiescent Current	$V_{\overline{SHDN}}$ = 2.5V, Not Switching			1.2	1.7	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
Reference Line Regulation	2.5V ≤ V_{IN} ≤ 40V			0.01	0.05	%/V
Switching Frequency, f_{OSC}	R_T = 56.2k R_T = 422k	● ●	1.23 165	1.5 200	1.77 235	MHz kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/6		Ratio
Switching Frequency Set Range	SYNCing or Free Running	●	200		1500	kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		35		65	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
Minimum Off-Time				100		ns
Minimum On-Time				120		ns
Switch Current Limit	Minimum Duty Cycle (Note 3) Maximum Duty Cycle (Notes 3, 4), f_{OSC} = 1.5MHz Maximum Duty Cycle (Notes 3, 4), f_{OSC} = 200kHz	● ● ●	1.2 0.6 0.4	1.5 1 0.8	1.8 1.5 1.4	A A A
Switch V_{CESAT}	I_{SW} = 0.75A			400		mV
Switch Leakage Current	V_{SW} = 5V			0.01	1	µA
Soft-Start Charging Current	V_{SS} = 0.5V	●	4	6	8	µA
$\overline{SHDN}$ Minimum Input Voltage High	Active Mode, $\overline{SHDN}$ Rising Active Mode, $\overline{SHDN}$ Falling	● ●	1.23 1.21	1.31 1.27	1.4 1.33	V V
$\overline{SHDN}$ Input Voltage Low	Shutdown Mode	●			0.3	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 1.3V $V_{\overline{SHDN}}$ = 0V		 9	44 12 0	56 15 0.1	µA µA µA
$\overline{SHDN}$ Hysteresis				40		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8580E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8580I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8580H is guaranteed over the full –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

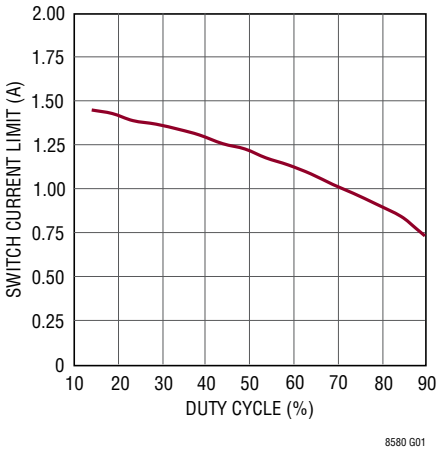
Note 3: Current limit guaranteed by design and/or correlation to static test.

Note 4: Current limit measured at equivalent of listed switching frequency.

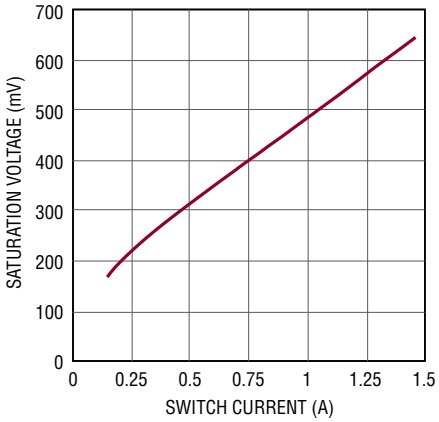
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified

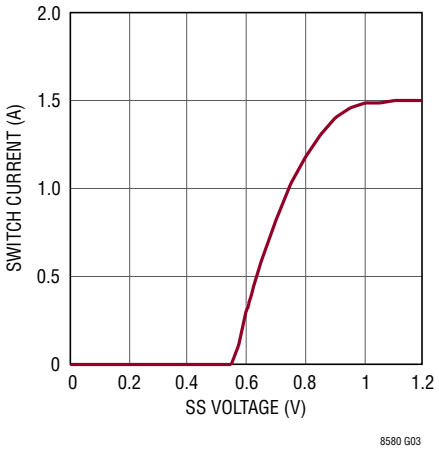
Switch Current Limit vs Duty Cycle



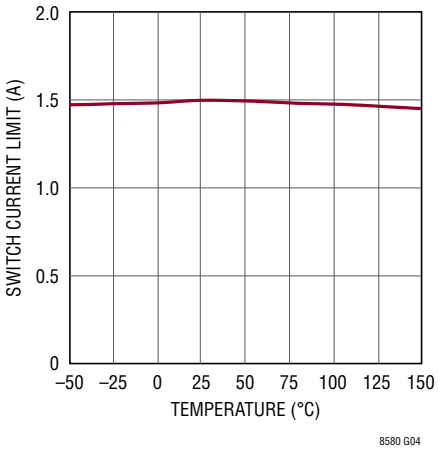
Switch Saturation Voltage



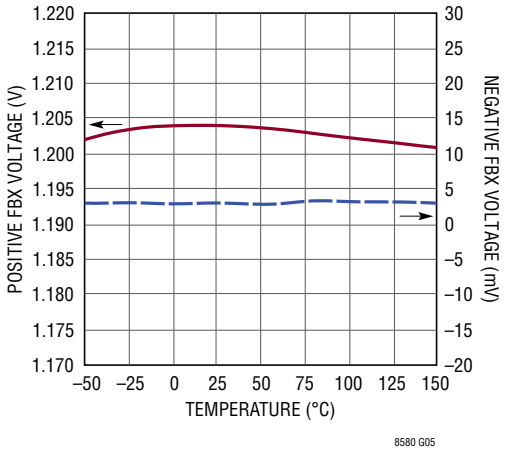
Commanded Switch Current vs SS



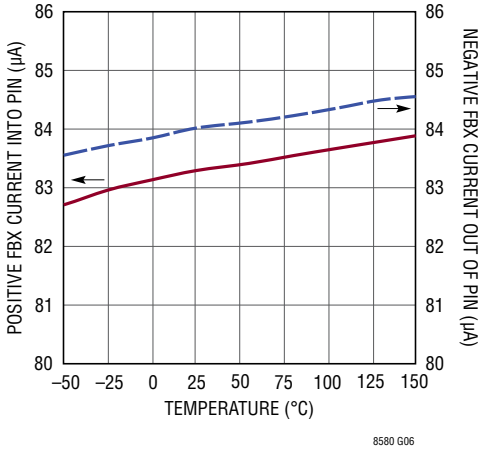
Switch Current Limit vs Temperature



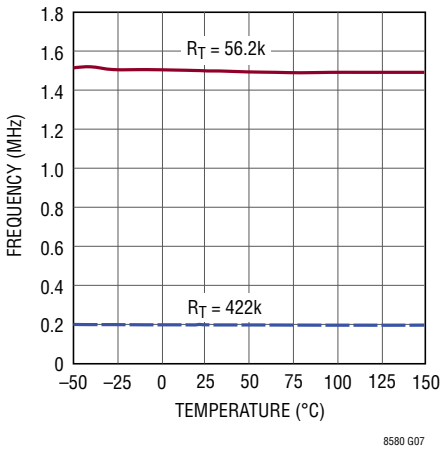
Positive and Negative Output Voltage Regulation



Positive and Negative FBX Current at Output Voltage Regulation

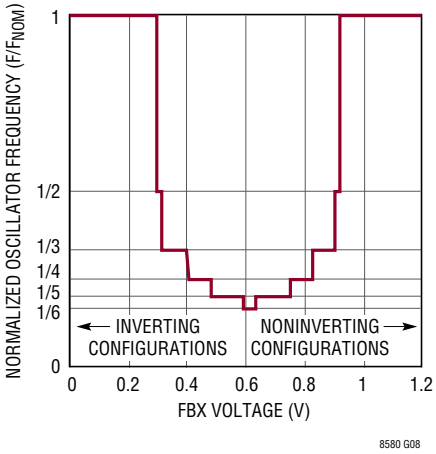


Oscillator Frequency

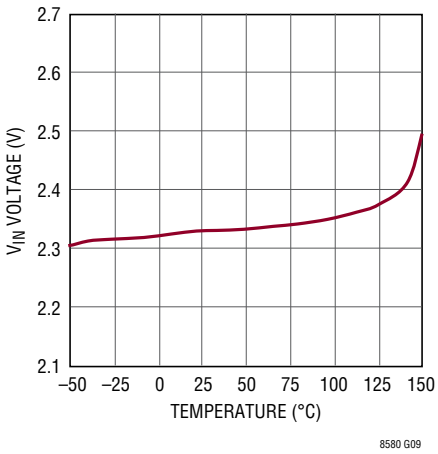


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified

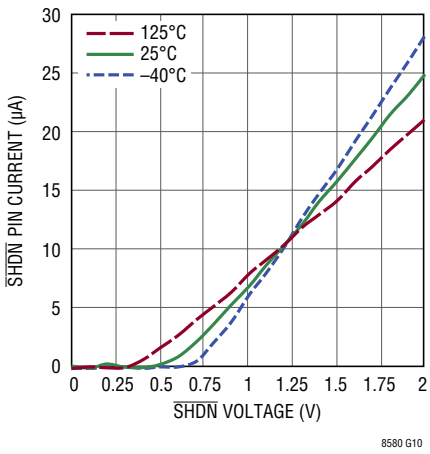
Oscillator Frequency During Soft-Start



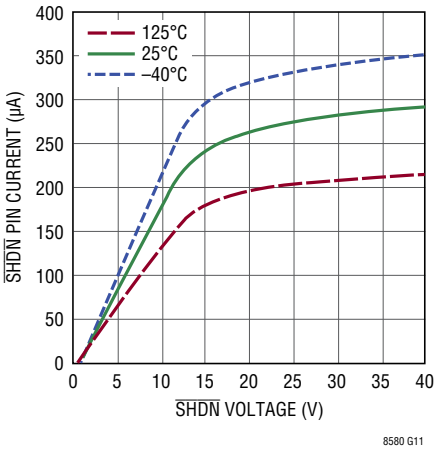
Internal UVLO



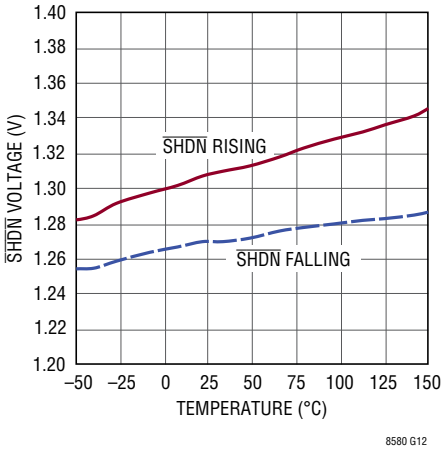
$\overline{SHDN}$ Pin Current



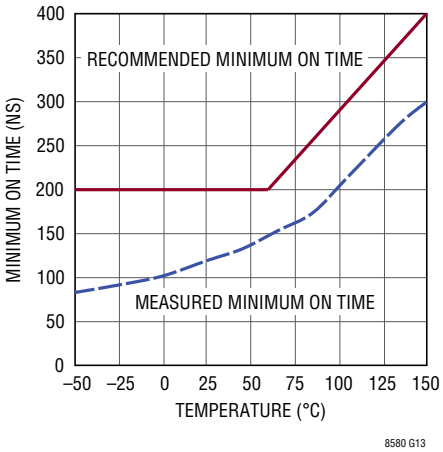
$\overline{SHDN}$ Pin Current



Active/Lockout Threshold



Minimum On Time vs Temperature



PIN FUNCTIONS

FBX (Pin 1): Positive and Negative Feedback Pin. For a noninverting or inverting converter, tie a resistor from the FBX pin to V_{OUT} according to the following equations:

$$R_{FBX} = \frac{(V_{OUT} - 1.204V)}{83.3\mu A}; \text{ Noninverting Converter}$$

$$R_{FBX} = \frac{(|V_{OUT}| + 3mV)}{83.3\mu A}; \text{ Inverting Converter}$$

VC (Pin 2): Error Amplifier Output Pin. Tie external compensation network to this pin.

V_{IN} (Pin 3): Input Supply Pin. Must be locally bypassed.

SW (Pin 4): Switch Pin. This is the collector of the internal NPN Power switch. Minimize the metal trace area connected to this pin to minimize EMI.

$\overline{SHDN}$ (Pin 5): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. Drive below 1.21V to disable the chip. Drive above 1.40V to activate the chip and restart the soft-start sequence. Do not float this pin.

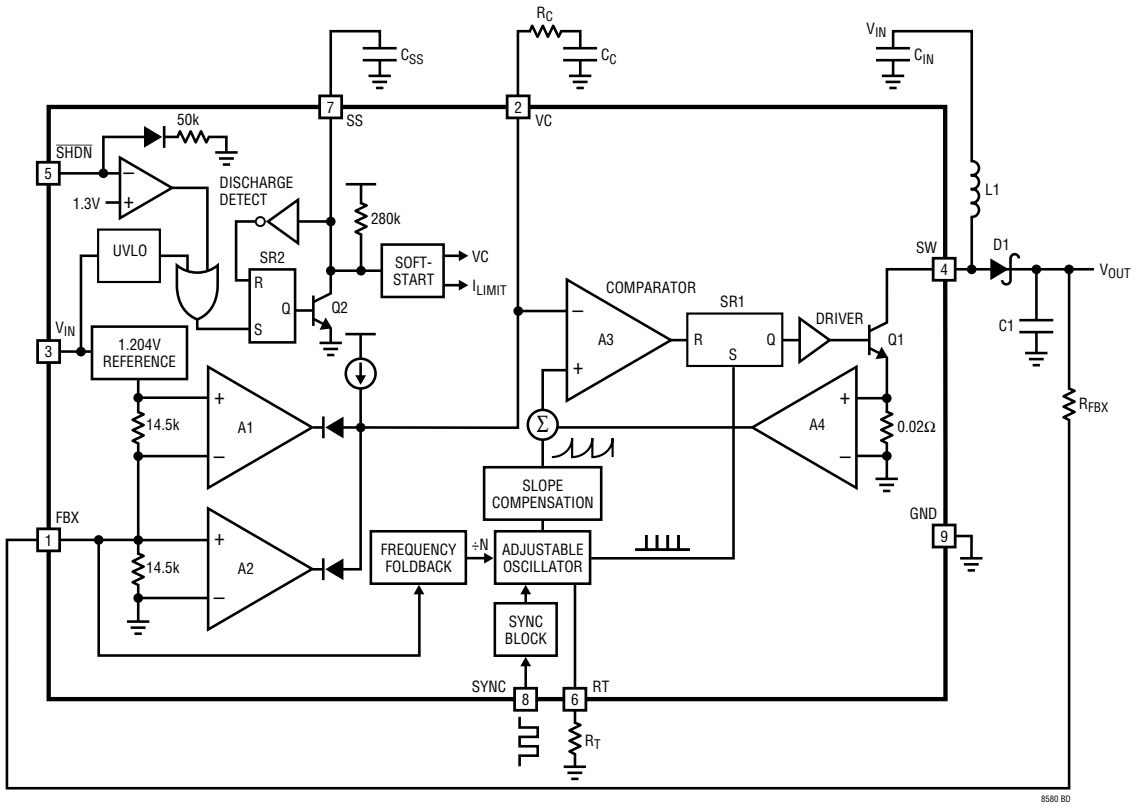
RT (Pin 6): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free running level. Do not float this pin.

SS (Pin 7): Soft-Start Pin. Place a soft-start capacitor here. Upon start-up, the SS pin will be charged by a (nominally) 280k resistor to about 2.1V.

SYNC (Pin 8): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less 0.4V. Drive this pin to less than 0.4V to revert to the internal free-running clock. See the Applications Information section for more information.

GND (Exposed Pad Pin 9): Ground. Exposed pad must be soldered directly to local ground plane.

BLOCK DIAGRAM



OPERATION

The LT8580 uses a constant-frequency, current mode control scheme to provide excellent line and load regulation. Refer to the Block Diagram for the following description of the part's operation. At the start of each oscillator cycle, the SR latch (SR1) is set, which turns on the power switch, Q1. The switch current flows through the internal current sense resistor, generating a voltage proportional to the switch current. This voltage (amplified by A4) is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When this voltage exceeds the level at the negative input of A3, the SR latch is reset, turning off the power switch. The level at the negative input of A3 (VC pin) is set by the error amplifier A1 (or A2) and is simply an amplified version of the difference between the feedback voltage (FBX pin) and the reference voltage (1.204V or 3mV, depending on the configuration). In this manner, the error amplifier sets the correct peak current level to keep the output in regulation.

The LT8580 has an FBX pin architecture that can be used for either noninverting or inverting configurations. When configured as a noninverting converter, the FBX pin is pulled up to the internal bias voltage of 1.204V by the R_{FBX} resistor connected from V_{OUT} to FBX. Amplifier A2 becomes inactive and amplifier A1 performs the inverting amplification from FBX to VC. When the LT8580 is in an inverting configuration, the FBX pin is pulled down to 3mV by the R_{FBX} resistor connected from V_{OUT} to FBX. Amplifier A1 becomes inactive and amplifier A2 performs the noninverting amplification from FBX to VC.

SEPIC Topology

As shown in Figure 1, the LT8580 can be configured as a SEPIC (single-ended primary inductance converter). This topology allows for the input to be higher, equal, or lower than the desired output voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output. This is useful for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

Inverting Topology

The LT8580 can also work in a dual inductor inverting topology, as shown in Figure 2. The part's unique feedback pin allows for the inverting topology to be built by simply changing the connection of external components. This solution results in very low output voltage ripple due to the inductor L2 in series with the output. Abrupt changes in output capacitor current are eliminated because the output inductor delivers current to the output during both the off-time and the on-time of the LT8580 switch.

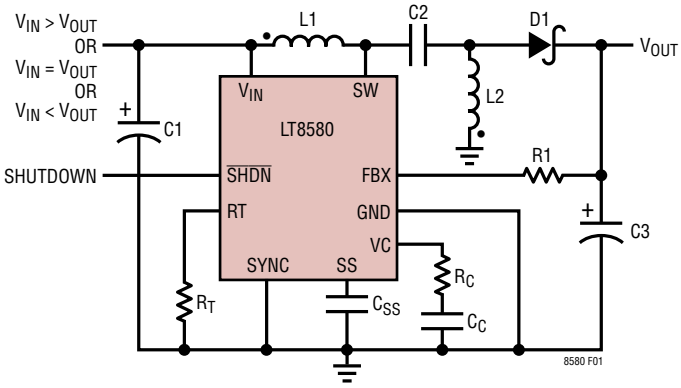


Figure 1. SEPIC Topology Allows for the Input to Span the Output Voltage. Coupled or Uncoupled Inductors Can Be Used. Follow Noted Phasing if Coupled

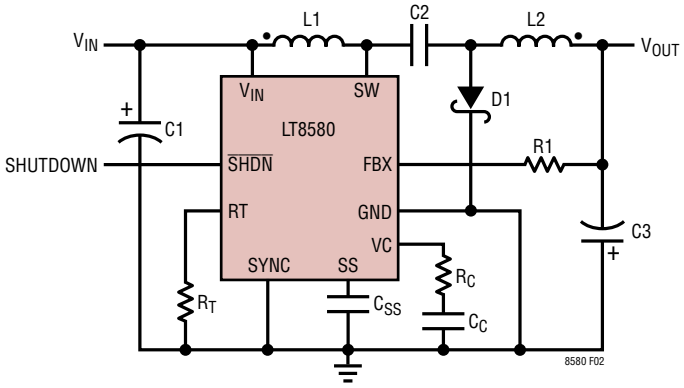


Figure 2. Dual Inductor Inverting Topology Results in Low Output Ripple. Coupled or Uncoupled Inductors Can Be Used. Follow Noted Phasing if Coupled

OPERATION

Start-Up Operation

Several functions are provided to enable a very clean start-up for the LT8580.

- First, the $\overline{SHDN}$ pin voltage is monitored by an internal voltage reference to give a precise turn-on voltage level. An external resistor (or resistor divider) can be connected from the input power supply to the $\overline{SHDN}$ pin to provide a user-programmable undervoltage lockout function.
- Second, the soft-start circuitry provides for a gradual ramp-up of the switch current. When the part is brought out of shutdown, the external SS capacitor is first discharged (providing protection against $\overline{SHDN}$ pin glitches and slow ramping), then an integrated 280k resistor pulls the SS pin up to ~2.1V. By connecting an external capacitor to the SS pin, the voltage ramp rate on the pin can be set. Typical values for the soft-start capacitor range from 100nF to 1µF.
- Finally, the frequency foldback circuit reduces the switching frequency when the FBX pin is in a nominal range of 300mV to 920mV. This feature reduces the minimum duty cycle that the part can achieve thus allowing better control of the switch current during start-up. When the FBX voltage is pulled outside of this range, the switching frequency returns to normal.

Current Limit and Thermal Shutdown Operation

The LT8580 has a current limit circuit not shown in the Block Diagram. The switch current is constantly monitored and not allowed to exceed the maximum switch current at a given duty cycle (see the Electrical Characteristics table). If the switch current reaches this value, the SR latch (SR1) is reset regardless of the state of the comparator (A1/A2). Also, not shown in the Block Diagram is the thermal shutdown circuit. If the temperature of the part exceeds approximately 165°C, the SR2 latch is set regardless of the state of the amplifier (A1/A2). When the part temperature falls below approximately 160°C, a full soft-start cycle will then be initiated. The current limit and thermal shutdown circuits protect the power switch as well as the external components connected to the LT8580.

APPLICATIONS INFORMATION

Setting Output Voltage

The output voltage is set by connecting a resistor (R_{FBX}) from V_{OUT} to the FBX pin. R_{FBX} is determined from the following equation:

$$R_{FBX} = \frac{|V_{OUT} - V_{FBX}|}{83.3\mu A}$$

where V_{FBX} is 1.204V (typical) for noninverting topologies (i.e., boost and SEPIC regulators) and 3mV (typical) for inverting topologies (see the Electrical Characteristics).

Power Switch Duty Cycle

In order to maintain loop stability and deliver adequate current to the load, the power NPN (Q1 in the Block Diagram) cannot remain "on" for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - \text{Min Off Time})}{T_P} \bullet 100\%$$

where T_P is the clock period and Min Off Time (found in the Electrical Characteristics) is typically 100ns.

The application should be designed so that the operating duty cycle does not exceed DC_{MAX}.

The minimum allowable duty cycle is given by:

$$DC_{MIN} = \frac{\text{Min On Time}}{T_P} \bullet 100\%$$

where T_P is the clock period and Minimum On Time is as shown in the Typical Performance Characteristics.

The application should be designed so that the operating duty cycle is at least DC_{MIN}.

Duty cycle equations for several common topologies are given below, where V_D is the diode forward voltage drop and V_{CESAT} is typically 400mV at 0.75A.

For the boost topology:

$$DC \cong \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC or dual inductor inverting topology (see Figure 1 and Figure 2):

$$DC \cong \frac{V_D + |V_{OUT}|}{V_{IN} + |V_{OUT}| + V_D - V_{CESAT}}$$

The LT8580 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

Inductor Selection

General Guidelines: The high frequency operation of the LT8580 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. To improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology, where each inductor only carries a fraction of the total switch current. Multilayer or chip inductors usually do not have enough core area to support peak inductor currents in the 1A to 2A range. To minimize radiated noise, use a toroidal or shielded inductor. Note that the inductance of shielded types will drop more as current increases, and will saturate more easily. See Table 1 for a list of inductor manufacturers. Thorough lab evaluation is recommended to verify that the following guidelines properly suit the final application.

Table 1. Inductor Manufacturers

Coilcraft	XAL5050, MSD7342, MSS7341 and LPS4018 Series	www.coilcraft.com
Coiltronics	DR, DRQ, LD and CD Series	www.coiltronics.com
Sumida	CDRH8D58/LD, CDRH64B, and CDRH70D430MN Series	www.sumida.com
Würth	WE-PD, WE-DD, WE-TPC, WE-LHMI and WE-LQS Series	www.we-online.com

Minimum Inductance: Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing

APPLICATIONS INFORMATION

an inductor, there are two conditions that limit the minimum inductance: (1) providing adequate load current, and (2) avoiding subharmonic oscillation. Choose an inductance that is high enough to meet both of these requirements.

Adequate Load Current: Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to a load (I_{OUT}). In order to provide adequate load current, L should be at least:

$$L_{BOOST} > \frac{DC \bullet V_{IN}}{2(f)\left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta}\right)}$$

for boost, topologies, or:

$$L_{DUAL} > \frac{DC \bullet V_{IN}}{2(f)\left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT}\right)}$$

for the SEPIC and inverting topologies.

where:

L_{BOOST} = L1 for boost topologies (see Figure 15)

L_{DUAL} = L1 = L2 for coupled dual inductor topologies (see Figure 16 and Figure 17)

L_{DUAL} = L1||L2 for uncoupled dual inductor topologies (see Figure 16 and Figure 17)

DC = switch duty cycle (see previous section)

I_{LIM} = switch current limit, typically about 1.2A at 50% duty cycle (see the Typical Performance Characteristics section).

η = power conversion efficiency (typically 85% for boost and 83% for dual inductor topologies at high currents).

f = switching frequency

I_{OUT} = maximum load current

Negative values of L indicate that the output load current I_{OUT} exceeds the switch current limit capability of the LT8580.

Avoiding Subharmonic Oscillations: The LT8580's internal slope compensation circuit can prevent subharmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} > \frac{V_{IN}}{1.25 \bullet (DC - 300ns \bullet f) \bullet f} \bullet \frac{2 \bullet DC - 1}{1 - DC}$$

L_{MIN} = L1 for boost topologies (see Figure 15)

L_{MIN} = L1 = L2 for coupled dual inductor topologies (see Figure 16 and Figure 17)

L_{MIN} = L1||L2 for uncoupled dual inductor topologies (see Figure 16 and Figure 17)

Maximum Inductance: Excessive inductance can reduce current ripple to levels that are difficult for the current comparator (A3 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} = \frac{V_{IN} - V_{CESAT}}{I_{MIN\text{-}RIPPLE}} \bullet \frac{DC}{f}$$

where

L_{MIN} = L1 for boost topologies (see Figure 15)

L_{MIN} = L1 = L2 for coupled dual inductor topologies (see Figure 16 and Figure 17)

L_{MIN} = L1||L2 for uncoupled dual inductor topologies (see Figure 16 and Figure 17)

$I_{MIN(RIPPLE)}$ = typically 80mA

Current Rating: Finally, the inductor(s) must have a rating greater than its peak operating current to prevent inductor saturation resulting in efficiency loss. In steady state, the peak input inductor current (continuous conduction mode only) is given by:

$$I_{L1\text{-}PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{IN} \bullet \eta} + \frac{V_{IN} \bullet DC}{2 \bullet L1 \bullet f}$$

for the boost, SEPIC and dual inductor inverting topologies.

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For dual dual inductor topologies, the peak output inductor current is given by:

$$I_{L2\text{-}PEAK} = I_{OUT} + \frac{|V_{OUT}| \bullet (1 - DC)}{2 \bullet L2 \bullet f}$$

For the dual inductor topologies, the total peak current is:

$$I_{L\text{-}PEAK} = I_{OUT}\left[1 + \frac{V_{OUT}}{\eta \bullet V_{IN}}\right] + \frac{V_{IN} \bullet DC}{2 \bullet L \bullet f}$$

Note: Peak inductor current is limited by the switch current limit. Refer to the Electrical Characteristics table and to the Switch Current Limit vs Duty Cycle plot in the Typical Performance Characteristics.

Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wider voltage and temperature ranges. A 0.47µF to 10µF output capacitor is sufficient for most applications. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than a ceramic and will have a higher ESR with greater output ripple.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as closely as possible to the V_{IN} pin of the LT8580 as well as to the inductor connected to the input of the power path. If it is not possible to optimally place a single input capacitor, then use one at the V_{IN} pin of the chip (C_{VIN}) and one at the input of the power path (C_{PWR}). See equations in Table 4, Table 5 and Table 6 for sizing information. A 1µF to 2.2µF input capacitor is sufficient for most applications.

Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 2. Ceramic Capacitor Manufacturers

Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
TDK	www.tdk.com

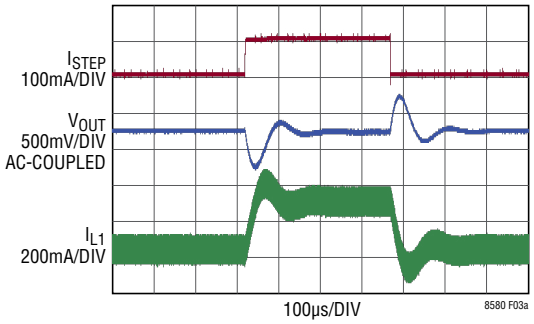
Compensation—Adjustment

To compensate the feedback loop of the LT8580, a series resistor-capacitor network in parallel with a single capacitor should be connected from the VC pin to GND. For most applications, the series capacitor should be in the range of 470pF to 2.2nF with 1nF being a good starting value. The parallel capacitor should range in value from 10pF to 100pF with 47pF a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k. A good technique to compensate a new application is to use a 100kΩ potentiometer in place of series resistor R_C. With the series capacitor and parallel capacitor at 1nF and 47pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. Figure 3 (3a to 3c) illustrates this process for the circuit of Figure 4 with a load current stepped between 60mA and 160mA. Figure 3a shows the transient response with R_C equal to 2k. The phase margin is poor, as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 3b, the value of R_C is increased to 3k, which results in a more damped response. Figure 3c shows the results when R_C is increased further to 6.04k. The transient response is nicely damped and the compensation procedure is complete.

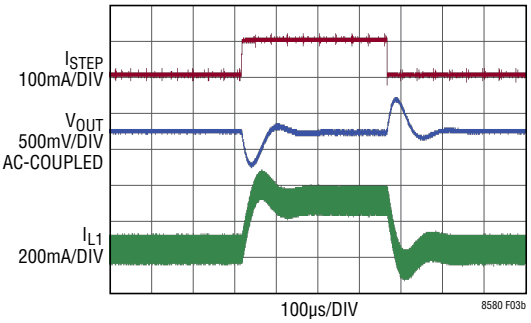
Compensation—Theory

Like all other current mode switching regulators, the LT8580 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT8580—a fast current loop which does not require compensation, and a slower voltage loop which does. Standard bode plot analysis can be used to understand and adjust the voltage feedback loop.

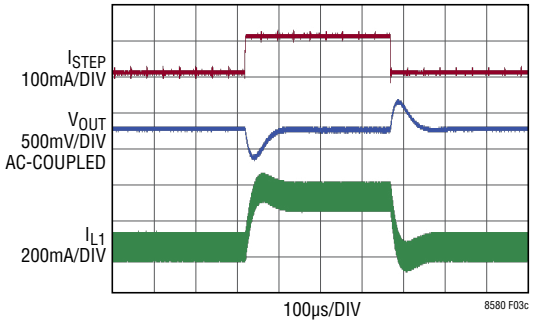
APPLICATIONS INFORMATION



(3a) Transient Response Shows Excessive Ringing



(3b) Transient Response Is Better



(3c) Transient Response Is Well Damped

Figure 3. Transient Response

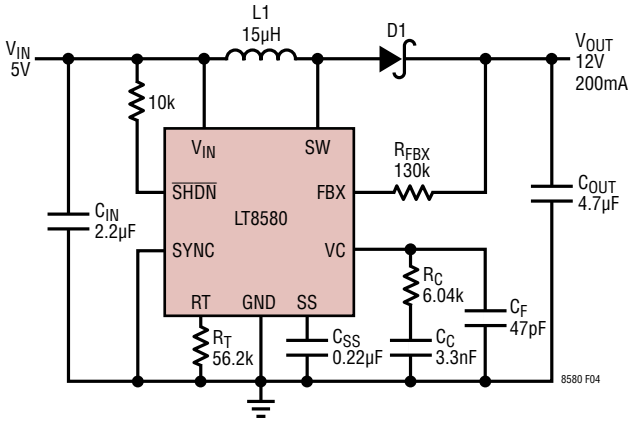
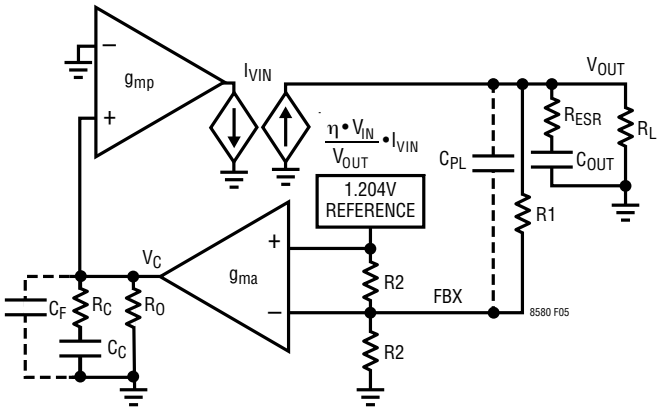


Figure 4. 1.5MHz, 5V to 12V Boost Converter

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As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 5 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source which converts I_{VIN} to $(\eta V_{IN}/V_{OUT}) \bullet I_{VIN}$. g_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the VC voltage. η is the efficiency of the switching regulator, and is typically about 85%.

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The limits for g_{mp} are in the Electrical Characteristics section (switch current limit), and g_{ma} is nominally limited to about +15µA and –17µA.



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS V_{OUT} DIVIDED BY $I_{LOAD(MAX)}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R1, R2: FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR
η: CONVERTER EFFICIENCY (~85% AT HIGHER CURRENTS)

Figure 5. Boost Converter Equivalent Model

From Figure 5, the DC gain, poles and zeros can be calculated as follows:

$$\text{Output Pole:} \quad P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole:} \quad P2 = \frac{1}{2 \bullet \pi \bullet [R_O + R_C] \bullet C_C}$$

$$\text{Error Amp Zero:} \quad Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

DC Gain:

(Breaking Loop at FBX Pin)

$$A_{DC} = A_{OL}(0) = \frac{\partial V_C}{\partial V_{FBX}} \bullet \frac{\partial I_{VIN}}{\partial V_C} \bullet \frac{\partial V_{OUT}}{\partial I_{VIN}} \bullet \frac{\partial V_{FBX}}{\partial V_{OUT}} =$$

$$(g_{ma} \bullet R_O) \bullet g_{mp} \bullet \left(\eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2}\right) \bullet \frac{0.5R2}{R1 + 0.5R2}$$

$$\text{ESR Zero:} \quad Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

$$\text{RHP Zero:} \quad Z3 = \frac{V_{IN}^2 \bullet R_L}{4 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

$$\text{High Frequency Pole:} \quad P3 > \frac{f_S}{3}$$

$$\text{Phase Lead Zero:} \quad Z4 = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{PL}}$$

$$\text{Phase Lead Pole:} \quad P4 = \frac{1}{2 \bullet \pi \bullet \frac{R1 \bullet \frac{R2}{2}}{R1 + \frac{R2}{2}} \bullet C_{PL}}$$

Error Amp Filter Pole:

$$P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

The current mode zero (Z3) is a right-half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

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Using the circuit in Figure 4 as an example, Table 3 shows the parameters used to generate the bode plot shown in Figure 6.

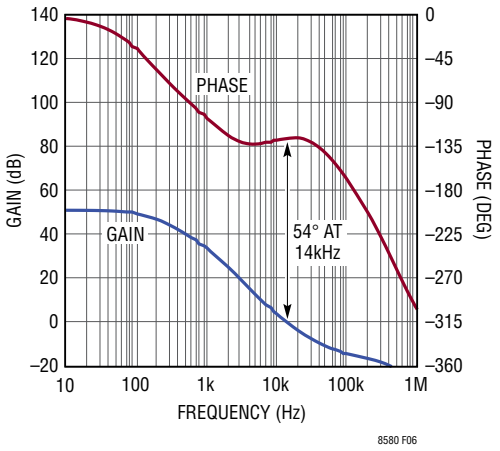


Figure 6. Bode Plot for Example Boost Converter

Table 3. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	60	Ω	Application Specific
C_{OUT}	4.7	µF	Application Specific
R_{ESR}	10	mΩ	Application Specific
R_O	300	kΩ	Not Adjustable
C_C	3300	pF	Adjustable
C_F	47	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	6.04	kΩ	Adjustable
R1	130	kΩ	Adjustable
R2	14.6	kΩ	Not Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	200	µmho	Not Adjustable
g_{mp}	7	mho	Not Adjustable
L	15	µH	Application Specific
f_S	1.5	MHz	Adjustable

In Figure 6, the phase is –126° when the gain reaches 0dB giving a phase margin of 54°. The crossover frequency is 14kHz, which is more than three times lower than the frequency of the RHP zero to achieve adequate phase margin.

Diode Selection

Schottky diodes, with their low forward-voltage drops and fast switching speeds, are recommended for use with the LT8580. For applications where V_R (see Tables 4, 5 and 6) < 40V, the Diodes, Inc. SBR1V40LP is a good choice. Where V_R > 40V, the Diodes Inc. DFLS1100 works well. These diodes are rated to handle an average forward current of 1A.

Oscillator

The operating frequency of the LT8580 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from R_T to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{85.5}{(R_T + 1)}$$

where f_{OSC} is in MHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in MHz) using:

$$R_T = \frac{85.5}{f_{OSC}} - 1$$

Clock Synchronization

The operating frequency of the LT8580 can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal into the SYNC pin. The LT8580 will operate at the SYNC clock frequency. The LT8580 will revert to the internal free-running oscillator clock after SYNC is driven low for a few free-running clock periods.

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Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see the Block Diagram). As a result, the switching operation of the LT8580 will stop.

The duty cycle of the SYNC signal must be between 35% and 65% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

(1) SYNC may not toggle outside the frequency range of 200kHz to 1.5MHz unless it is stopped low to enable the free-running oscillator.

(2) The SYNC frequency can always be higher than the free-running oscillator frequency, f_{OSC}, but should not be less than 25% below f_{OSC}.

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz, and in that case, a 1.5MHz switching converter frequency may be employed. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade-off is efficiency, since the switching losses due to NPN base charge (see Thermal Calculations), Schottky diode charge, and other capacitive loss terms increase proportionally with frequency.

Soft-Start

The LT8580 contains a soft-start circuit to limit peak switch currents during start-up. High start-up current is inherent in switching regulators in general since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible, which results in large peak currents.

The start-up current can be limited by connecting an external capacitor (typically 100nF to 1µF) to the SS pin. This capacitor is slowly charged to ~2.1V by an internal 280k resistor once the part is activated. SS pin voltages below ~1.1V reduce the internal current limit. Thus, the gradual ramping of the SS voltage also gradually increases the current limit as the capacitor charges. This, in turn, allows the output capacitor to charge gradually toward its final value while limiting the start-up current.

In the event of a commanded shutdown or lockout ($\overline{SHDN}$ pin), internal undervoltage lockout (UVLO) or a thermal lockout, the soft-start capacitor is automatically discharged to ~200mV before charging resumes, thus assuring that the soft-start occurs after every reactivation of the chip.

Shutdown

The $\overline{SHDN}$ pin is used to enable or disable the chip. For most applications, $\overline{SHDN}$ can be driven by a digital logic source. Voltages above 1.4V enable normal active operation. Voltages below 300mV will shutdown the chip, resulting in extremely low quiescent current.

While the $\overline{SHDN}$ voltage transitions through the lockout voltage range (0.3V to 1.21V) the power switch is disabled and the SR2 latch is set (see the Block Diagram). This causes the soft-start capacitor to begin discharging, which continues until the capacitor is discharged and active operation is enabled. Although the power switch is disabled, $\overline{SHDN}$ voltages in the lockout range do not necessarily reduce quiescent current until the $\overline{SHDN}$ voltage is near or below the shutdown threshold.

Also note that $\overline{SHDN}$ can be driven above V_{IN} or V_{OUT} as long as the $\overline{SHDN}$ voltage is limited to less than 40V.

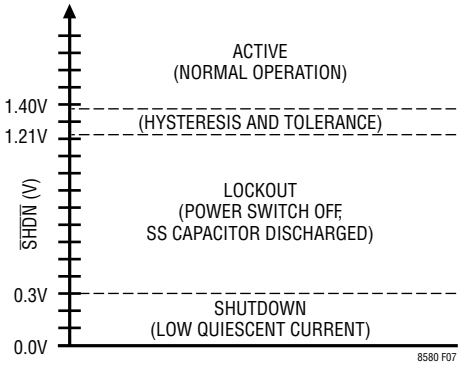


Figure 7. Chip States vs $\overline{SHDN}$ Voltage

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Configurable Undervoltage Lockout

Figure 8 shows how to configure an undervoltage lockout (UVLO) for the LT8580. Typically, UVLO is used in situations where the input supply is current-limited, has a relatively high source resistance, or ramps up/down slowly. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current-limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

The shutdown pin comparator has voltage hysteresis with typical thresholds of 1.31V (rising) and 1.27V (falling). Resistor R_{UVLO2} is optional. R_{UVLO2} can be included to reduce the overall UVLO voltage variation caused by variations in $\overline{SHDN}$ pin current (see the Electrical Characteristics). A good choice for R_{UVLO2} is ≤10k ±1%. After choosing a value for R_{UVLO2}, R_{UVLO1} can be determined from either of the following:

$$R_{UVLO1} = \frac{V_{IN}^{+} - 1.31V}{\left(\frac{1.31V}{R_{UVLO2}}\right) + 12\mu A}$$

or

$$R_{UVLO1} = \frac{V_{IN}^{-} - 1.27V}{\left(\frac{1.27V}{R_{UVLO2}}\right) + 12\mu A}$$

where V_{IN}^{+} and V_{IN}^{-} are the V_{IN} voltages when rising or falling, respectively.

For example, to disable the LT8580 for V_{IN} voltages below 3.5V using the single resistor configuration, choose:

$$R_{UVLO1} = \frac{3.5V - 1.27V}{\left(\frac{1.27V}{\infty}\right) + 12\mu A} = 187k$$

To activate the LT8580 for V_{IN} voltages greater than 4.5V using the double resistor configuration, choose R_{UVLO2} = 10k and:

$$R_{UVLO1} = \frac{4.5V - 1.31V}{\left(\frac{1.31V}{10k}\right) + 12\mu A} = 22.1k$$

Internal Undervoltage Lockout

The LT8580 monitors the V_{IN} supply voltage in case V_{IN} drops below a minimum operating level (typically about 2.35V). When V_{IN} is detected low, the power switch is deactivated, and while sufficient V_{IN} voltage persists, the soft-start capacitor is discharged. After V_{IN} is detected high, the power switch will be reactivated and the soft-start capacitor will begin charging.

Thermal Considerations

For the LT8580 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This is accomplished by taking advantage of the thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

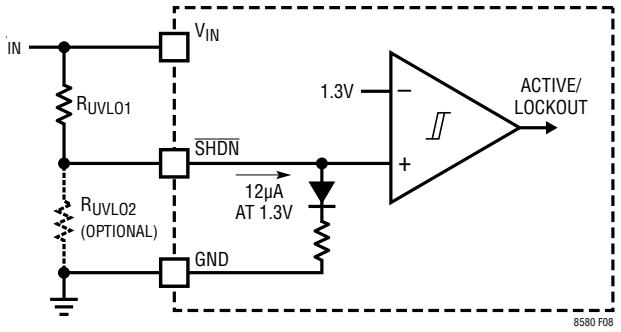


Figure 8. Configurable UVLO

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Thermal Lockout

If the die temperature reaches approximately 165°C, the part will go into thermal lockout, the power switch will be turned off and the soft-start capacitor will be discharged. The part will be enabled again when the die temperature has dropped by ~5°C (nominal).

Thermal Calculations

Power dissipation in the LT8580 chip comes from four primary sources: switch I^2R loss, NPN base drive (AC), NPN base drive (DC), and additional input current. The following formulas can be used to approximate the power losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency in discontinuous mode or at light load currents.

Average Input Current: $I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$

Switch Conduction Loss: $P_{SW} = (DC)(I_{IN})(V_{SW})$

Base Drive Loss (AC): $P_{BAC} = 20ns(I_{IN})(V_{OUT})(f)$

Base Drive Loss (DC): $P_{BDC} = \frac{(V_{IN})(I_{IN})(DC)}{40}$

Input Power Loss: $P_{INP} = 6mA\ (V_{IN})$

where:

V_{SW} = switch on voltage (see Typical Performance Characteristics for Switch Saturation Voltage)

DC = duty cycle (see the Power Switch Duty Cycle section for formulas)

η = power conversion efficiency (typically 85% at high currents)

Example: boost configuration, V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.2A, f = 1.25MHz, V_D = 0.5V:

I_{IN} = 0.56A

DC = 62.0%

P_{SW} = 117mW

P_{BAC} = 169mW

P_{BDC} = 44mW

P_{INP} = 30mW

Total LT8580 power dissipation (P_{TOT}) = 361mW

Thermal resistance for the LT8580 is influenced by the presence of internal, topside or backside planes. To calculate die temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$T_J = T_A + \theta_{JA} \bullet P_{TOT}$

where T_J = junction temperature, T_A = ambient temperature, and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The published θ_{JA} value is 43°C/W for the 3mm × 3mm DFN package and 35°C/W to 40°C/W for the MSOP exposed pad package. In practice, lower θ_{JA} values can be obtained if the board layout uses ground as a heat sink. For instance, thermal resistances of 34.7°C/W for the DFN package and 22.5°C/W for the MSOP package were obtained on a board designed with large ground planes.

V_{IN} Ramp Rate

While initially powering a switching converter application, the V_{IN} ramp rate should be limited. High V_{IN} ramp rates can cause excessive inrush currents in the passive components of the converter. This can lead to current and/or voltage overstress and may damage the passive components or the chip. Ramp rates less than 500mV/µs, depending on component parameters, will generally prevent these issues. Also, be careful to avoid hot-plugging. Hot-plugging occurs when an active voltage supply is "instantly" connected or switched to the input of the converter. Hot-plugging results in very fast input ramp rates and is not recommended. Finally, for more information, refer to Linear application note AN88, which discusses voltage overstress that can occur when an inductive source impedance is hot-plugged to an input pin bypassed by ceramic capacitors.

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Layout Hints

As with all high frequency switchers, when considering layout, care must be taken to achieve optimal electrical, thermal and noise performance. One will not get advertised performance with a careless layout. For maximum efficiency, switch rise and fall times are typically in the 10ns to 20ns range. To prevent noise, both radiated and conducted, the high speed switching current path, shown in Figure 9, must be kept as short as possible. This is implemented in the suggested layout of a boost configuration in Figure 10. Shortening this path will also reduce the parasitic trace inductance. At switch-off, this parasitic inductance produces a flyback spike across the LT8580 switch. When operating at higher currents and output voltages, with poor layout, this spike can generate voltages across the LT8580 that may exceed its absolute maximum rating. A ground plane should also be used under the switcher circuitry to prevent interplane coupling and overall noise.

The VC and FBX components should be kept as far away as practical from the switch node. The ground for these components should be separated from the switch current path. Failure to do so can result in poor stability or subharmonic oscillation.

Board layout also has a significant effect on thermal resistance. The exposed package ground pad is the copper plate that runs under the LT8580 die. This is a good thermal path for heat out of the package. Soldering the pad onto the board reduces die temperature and increases the power capability of the LT8580. Provide as much copper area as possible around this pad. Adding multiple feedthroughs around the pad to the ground plane will also help. Figure 10 and Figure 11 show the recommended component placement for the boost and SEPIC configurations, respectively.

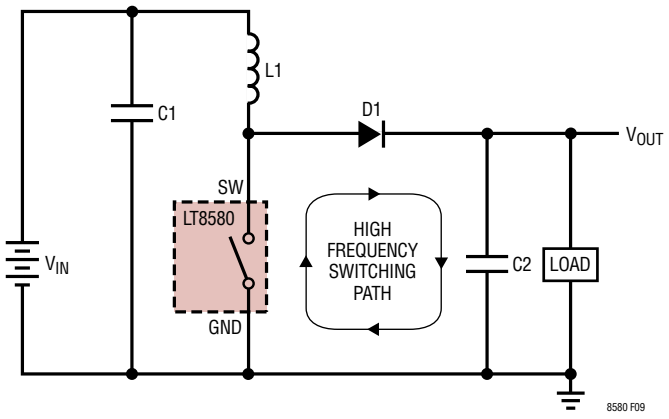


Figure 9. High Speed "Chopped" Switching Path for Boost Topology

Layout Hints for Inverting Topology

Figure 12 shows recommended component placement for the dual inductor inverting topology. Input bypass capacitor, C1, should be placed close to the LT8580, as shown. The load should connect directly to the output capacitor, C2, for best load regulation. The local ground may be tied into the system ground plane at the C3 ground terminal.

The cut ground copper at D1's cathode is essential to obtain low noise. This important layout issue arises due to the chopped nature of the currents flowing in Q1 and D1. If they are both tied directly to the ground plane before being combined, switching noise will be introduced into the ground plane. It is almost impossible to get rid of this noise, once present in the ground plane. The solution is to tie D1's cathode to the ground pin of the LT8580 before the combined currents are dumped in the ground plane as drawn in Figure 2, Figure 13 and Figure 14. This single layout technique can virtually eliminate high frequency "spike" noise, so often present on switching regulator outputs.

DIFFERENCES FROM LT3580

LT8580 is very similar to LT3580. However, LT8580 does deviate from LT3580 in a few areas:

- 65V, 1A switch
- 40V V_{IN} and $\overline{SHDN}$ absolute maximum rating
- FB renamed to FBX
- 5V FBX absolute maximum rating

APPLICATIONS INFORMATION

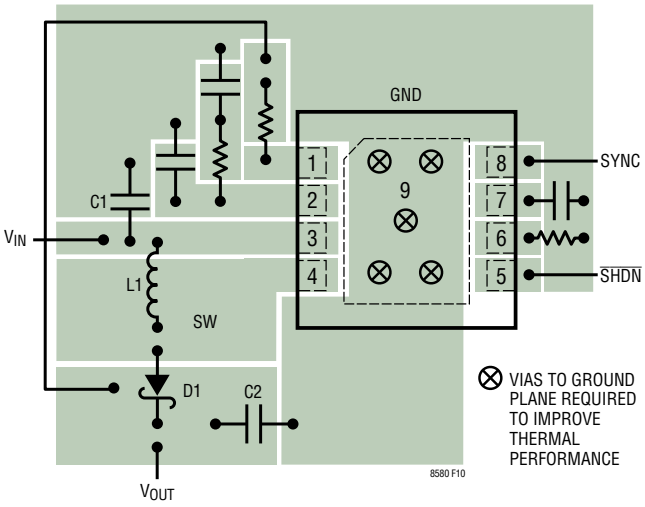


Figure 10. Suggested Component Placement for Boost Topology (Both DFN and MSOP Packages. Not to Scale). Pin 9 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

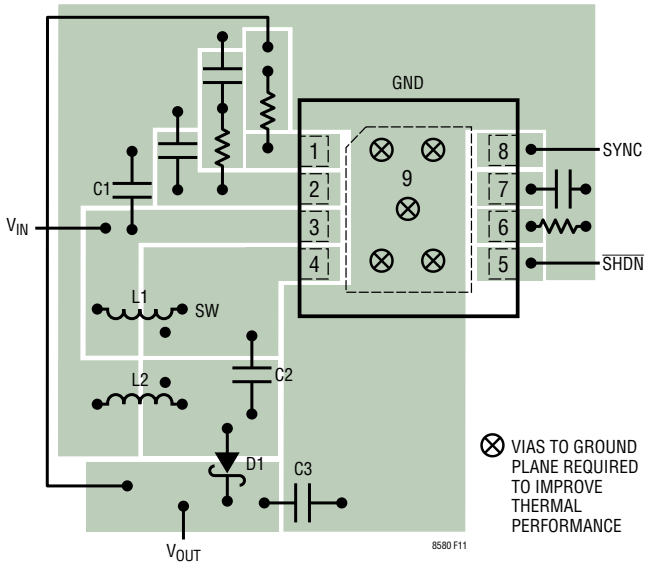


Figure 11. Suggested Component Placement for SEPIC Topology (Both DFN And MSOP Packages. Not to Scale). Pin 9 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

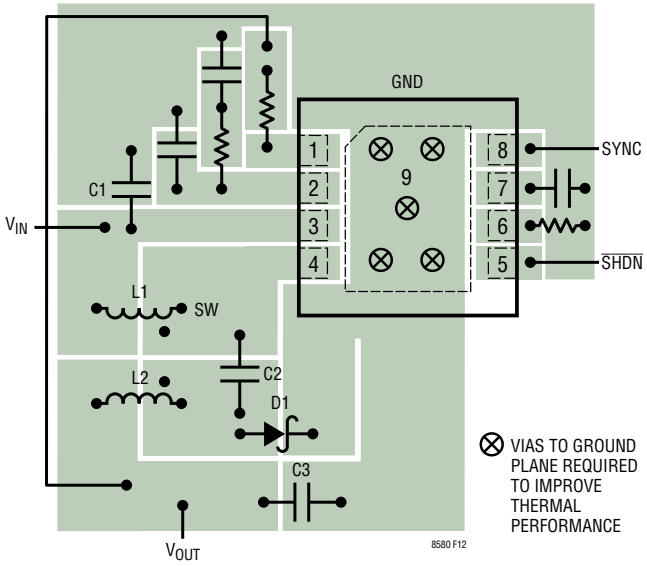


Figure 12. Suggested Component Placement for Inverting Topology (Both DFN and MSOP Packages. Not to Scale). Note Cut in Ground Copper at Diode's Cathode. Pin 9 (Exposed Pad) Must be Soldered Directly to Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

APPLICATIONS INFORMATION

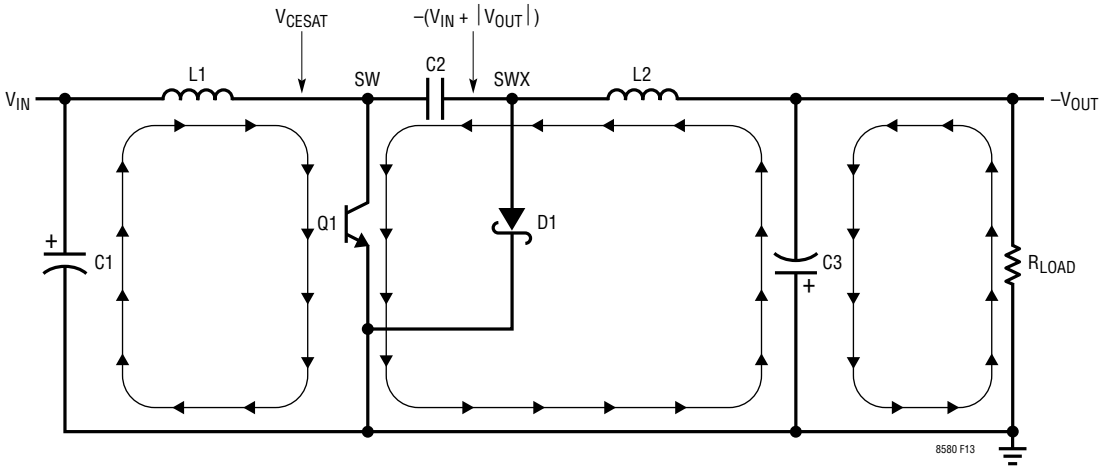


Figure 13. Switch-On Phase of an Inverting Converter. L1 and L2 Have Positive dI/dt

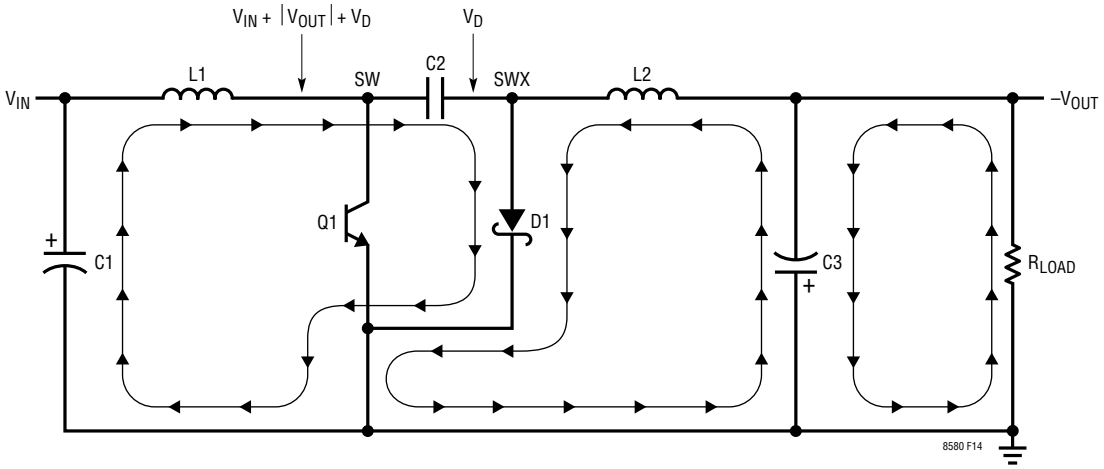


Figure 14. Switch-Off Phase of an Inverting Converter. L1 and L2 Currents Have Negative dI/dt

APPLICATIONS INFORMATION

BOOST CONVERTER COMPONENT SELECTION

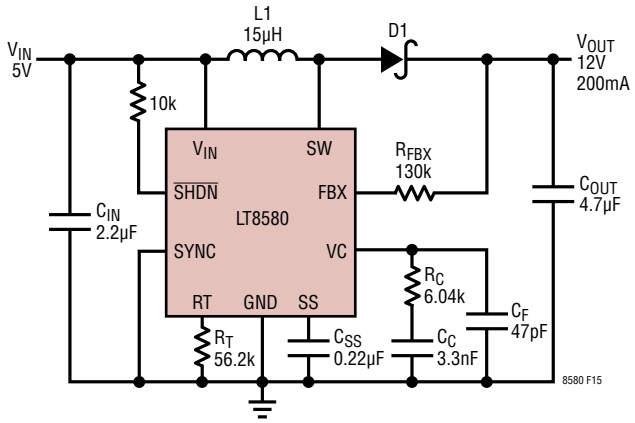


Figure 15. Boost Converter: The Component Values and Voltages Given Are Typical Values for a 1.5MHz, 5V to 12V Boost

The LT8580 can be configured as a boost converter as in Figure 15. This topology allows for positive output voltages that are higher than the input voltage. A single feedback resistor sets the output voltage. For output voltages higher than 60V, see the Charge Pump Aided Regulators section.

Table 4 is a step-by-step set of equations to calculate component values for the LT8580 when operating as a boost converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Applications Information section for further information on the design equations presented in Table 4.

Variable Definitions:

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

DC = Power Switch Duty Cycle

f_{OSC} = Switching Frequency

I_{OUT} = Maximum Average Output Current

I_{RIPPLE} = Inductor Ripple Current

Table 4. Boost Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below
Step 2: DC	$DC_{MAX} = \frac{V_{OUT} - V_{IN(MIN)} + 0.5\,V}{V_{OUT} + 0.5\,V - 0.4\,V}$ $DC_{MIN} = \frac{V_{OUT} - V_{IN(MAX)} + 0.5\,V}{V_{OUT} + 0.5\,V - 0.4\,V}$
Step 3: L1	$L_{TYP} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet 0.3\,A}$ (1) $L_{MIN} = \frac{(V_{IN(MIN)} - 0.4V) \bullet (2 \bullet DC_{MAX} - 1)}{1.25 \bullet (DC_{MAX} - 300ns \bullet f_{OSC}) \bullet f_{OSC} \bullet (1 - DC_{MAX})}$ (2) $L_{MAX1} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet 0.08\,A}$ (3) $L_{MAX2} = \frac{(V_{IN(MAX)} - 0.4V) \bullet DC_{MIN}}{f_{OSC} \bullet 0.08\,A}$ (4) • Solve equations 1 to 4 for a range of L values • The minimum of the L value range is the higher of L_{TYP} and L_{MIN} • The maximum of the L value range is the lower of L_{MAX1} and L_{MAX2}.
Step 4: I_{RIPPLE}	$I_{RIPPLE(MIN)} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet L_1}$ $I_{RIPPLE(MAX)} = \frac{(V_{IN(MAX)} - 0.4V) \bullet DC_{MIN}}{f_{OSC} \bullet L_1}$
Step 5: I_{OUT}	$I_{OUT(MIN)} = \left(1A - \frac{I_{RIPPLE(MIN)}}{2}\right) \bullet (1 - DC_{MAX})$ $I_{OUT(MAX)} = \left(1A - \frac{I_{RIPPLE(MAX)}}{2}\right) \bullet (1 - DC_{MIN})$
Step 6: D1	$V_R > V_{OUT}$; $I_{AVG} > I_{OUT}$
Step 7: C_{OUT}	$C_{OUT} \geq \frac{I_{OUT} \bullet DC_{MAX}}{f_{OSC} \bullet 0.005 \bullet V_{OUT}}$
Step 8: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq$ $\frac{1A \bullet DC_{MAX}}{40 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN(MIN)}} + \frac{I_{RIPPLE(MAX)}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN(MAX)}}$ • Refer to the Capacitor Selection Section for definition of C_{VIN} and C_{PWR}
Step 9: R_{FBX}	$R_{FBX} = \frac{V_{OUT} - 1.204V}{83.3\mu A}$
Step 10: R_T	$R_T = \frac{85.5}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note 1: This table uses 1A for the peak switch current. Refer to the Electrical Characteristics Table and Typical Performance Characteristics plots for the peak switch current at an operating duty cycle.

Note 2: The final values for C_{OUT} and C_{IN} may deviate from the previous equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

SEPIC CONVERTER COMPONENT SELECTION (COUPLED OR UNCOUPLED INDUCTORS)

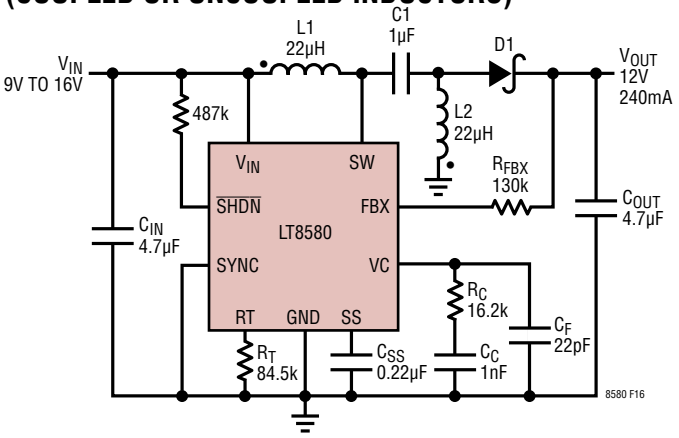


Figure 16. SEPIC Converter: The Component Values and Voltages Given Are Typical Values for a 1MHz, 9V to 16V Input to 12V Output SEPIC Converter

The LT8580 can also be configured as a SEPIC, as shown in Figure 16. This topology allows for positive output voltages that are lower, equal or higher than the input voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output due to capacitor C1.

Table 5 is a step-by-step set of equations to calculate component values for the LT8580 when operating as a SEPIC converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC}, respectively). Refer to the Applications Information section for further information on the design equations presented in Table 5.

Variable Definitions:

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

DC = Power Switch Duty Cycle

f_{OSC} = Switching Frequency

I_{OUT} = Maximum Average Output Current

I_{RIPPLE} = Inductor Ripple Current

Table 5. SEPIC Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT} and f_{OSC} to calculate equations below
Step 2: DC	$DC_{MAX} = \frac{V_{OUT} + 0.5\,V}{V_{IN(MIN)} + V_{OUT} + 0.5\,V - 0.4V}$ $DC_{MIN} = \frac{V_{OUT} + 0.5\,V}{V_{IN(MAX)} + V_{OUT} + 0.5\,V - 0.4V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet 0.3\,A}$ (1) $L_{MIN} = \frac{(V_{IN(MIN)} - 0.4V) \bullet (2 \bullet DC_{MAX} - 1)}{1.25 \bullet (DC_{MAX} - 300ns \bullet f_{OSC}) \bullet f_{OSC} \bullet (1 - DC_{MAX})}$ (2) $L_{MAX} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet 0.08\,A}$ (3) • Solve equations 1, 2 and 3 for a range of L values • The minimum of the L value range is the higher of L_{TYP} and L_{MIN} • The maximum of the L value range is L_{MAX} • L = L1 = L2 for coupled inductors • L = L1 || L2 for uncoupled inductors
Step 4: I_{RIPPLE}	$I_{RIPPLE(MIN)} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet L}$ $I_{RIPPLE(MAX)} = \frac{(V_{IN(MAX)} - 0.4V) \bullet DC_{MIN}}{f_{OSC} \bullet L}$
Step 5: I_{OUT}	$I_{OUT(MIN)} = \left(1A - \frac{I_{RIPPLE(MIN)}}{2}\right) \bullet (1 - DC_{MAX})$ $I_{OUT(MAX)} = \left(1A - \frac{I_{RIPPLE(MAX)}}{2}\right) \bullet (1 - DC_{MIN})$
Step 6: D1	$V_R > V_{IN} + V_{OUT}$; $I_{AVG} > I_{OUT}$
Step 7: C1	C1 ≥ 1µF; $V_{RATING} \geq V_{IN}$
Step 8: C_{OUT}	$C_{OUT} \geq \frac{I_{OUT(MIN)} \bullet DC_{MAX}}{f_{OSC} \bullet 0.005 \bullet V_{OUT}}$
Step 9: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq$ $\frac{1A \bullet DC_{MAX}}{40 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN(MIN)}} + \frac{I_{RIPPLE(MAX)}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN(MAX)}}$ • Refer to the Capacitor Selection Section for definition of C_{VIN} and C_{PWR}
Step 10: R_{FBX}	$R_{FBX} = \frac{V_{OUT} - 1.204V}{83.3\mu A}$
Step 11: R_T	$R_T = \frac{85.5}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note 1: This table uses 1A for the peak switch current. Refer to the Electrical Characteristics Table and Typical Performance Characteristics plots for the peak switch current at an operating duty cycle.

Note 2: The final values for C_{OUT}, C_{IN} and C1 may deviate from the previous equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

DUAL INDUCTOR INVERTING CONVERTER COMPONENT SELECTION (COUPLED OR UNCOUPLED INDUCTORS)

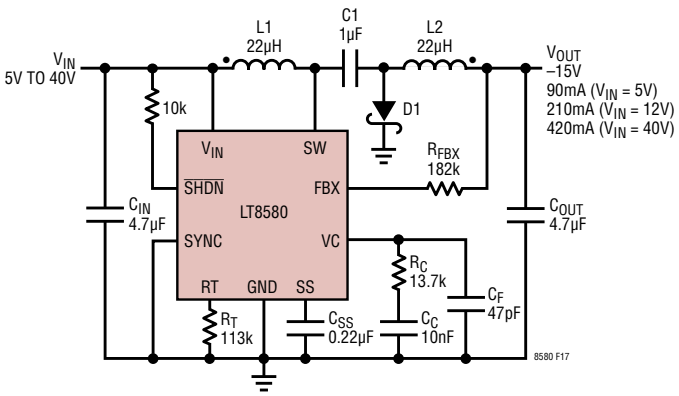


Figure 17. Dual Inductor Inverting Converter: The Component Values and Voltages Given Are Typical Values for a 750kHz Wide Input (5V to 40V) to –15V Inverting Topology Using Coupled Inductors

Due to its unique FBX pin, the LT8580 can work in a dual inductor inverting configuration as in Figure 17. Changing the connections of L2 and the Schottky diode in the SEPIC topology results in generating negative output voltages. This solution results in very low output voltage ripple due to inductor L2 being in series with the output. Output disconnect is inherently built into this topology due to the capacitor C1.

Table 6 is a step-by-step set of equations to calculate component values for the LT8580 when operating as a dual inductor inverting converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Applications Information section for further information on the design equations presented in Table 6.

Variable Definitions:

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

DC = Power Switch Duty Cycle

f_{OSC} = Switching Frequency

I_{OUT} = Maximum Average Output Current

I_{RIPPLE} = Inductor Ripple Current

Table 6. Dual Inductor Inverting Design Equations

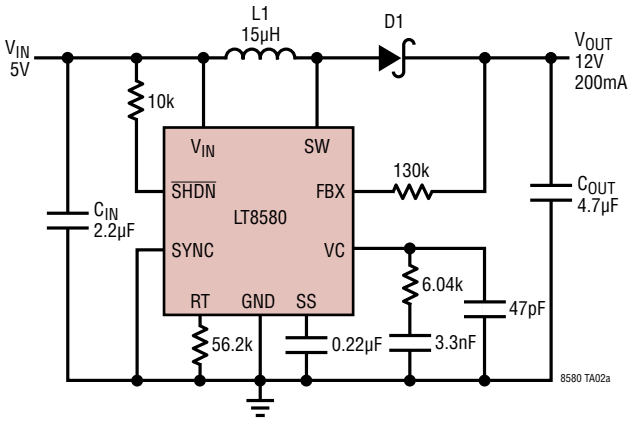
	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT} and f_{OSC} to calculate equations below
Step 2: DC	$DC_{MAX} = \frac{\lvert V_{OUT}\rvert + 0.5\,V}{V_{IN(MIN)} + \lvert V_{OUT}\rvert + 0.5\,V - 0.4\,V}$ $DC_{MIN} = \frac{\lvert V_{OUT}\rvert + 0.5\,V}{V_{IN(MAX)} + \lvert V_{OUT}\rvert + 0.5\,V - 0.4\,V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet 0.3\,A}$ (1) $L_{MIN} = \frac{(V_{IN(MIN)} - 0.4V) \bullet (2 \bullet DC_{MAX} - 1)}{1.25 \bullet (DC_{MAX} - 300ns \bullet f_{OSC}) \bullet f_{OSC} \bullet (1 - DC_{MAX})}$ (2) $L_{MAX} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet 0.08\,A}$ (3) • Solve equations 1, 2 and 3 for a range of L values • The minimum of the L value range is the higher of L_{TYP} and L_{MIN} • The maximum of the L value range is L_{MAX} • L = L1 = L2 for coupled inductors • L = L1 || L2 for uncoupled inductors
Step 4: I_{RIPPLE}	$I_{RIPPLE(MIN)} = \frac{(V_{IN(MIN)} - 0.4V) \bullet DC_{MAX}}{f_{OSC} \bullet L}$ $I_{RIPPLE(MAX)} = \frac{(V_{IN(MAX)} - 0.4V) \bullet DC_{MIN}}{f_{OSC} \bullet L}$
Step 5: I_{OUT}	$I_{OUT(MIN)} = \left(1A - \frac{I_{RIPPLE(MIN)}}{2}\right) \bullet (1 - DC_{MAX})$ $I_{OUT(MAX)} = \left(1A - \frac{I_{RIPPLE(MAX)}}{2}\right) \bullet (1 - DC_{MIN})$
Step 6: D1	$V_R > V_{IN} + \lvert V_{OUT}\rvert$; $I_{AVG} > I_{OUT}$
Step 7: C1	C1 ≥ 1µF; $V_{RATING} \geq V_{IN(MAX)} + \lvert V_{OUT}\rvert$
Step 8: C_{OUT}	$C_{OUT} \geq \frac{I_{RIPPLE(MAX)}}{8 \bullet f_{OSC}\,(0.005 \bullet \lvert V_{OUT}\rvert)}$
Step 9: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq$ $\frac{1A \bullet DC_{MAX}}{40 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN(MIN)}} + \frac{I_{RIPPLE(MAX)}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN(MAX)}}$ • Refer to the Capacitor Selection Section for definition of C_{VIN} and C_{PWR}
Step 10: R_{FBX}	$R_{FBX} = \frac{\lvert V_{OUT}\rvert + 3mV}{83.3\mu A}$
Step 11: R_T	$R_T = \frac{85.5}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note 1: This table uses 1A for the peak switch current. Refer to the Electrical Characteristics Table and Typical Performance Characteristics plots for the peak switch current at an operating duty cycle.

Note 2: The final values for C_{OUT}, C_{IN} and C1 may deviate from the previous equations in order to obtain desired load transient performance.

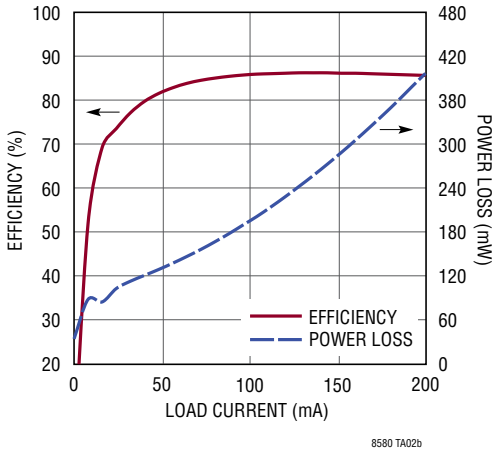
TYPICAL APPLICATIONS

1.5MHz, 5V to 12V Output Boost Converter

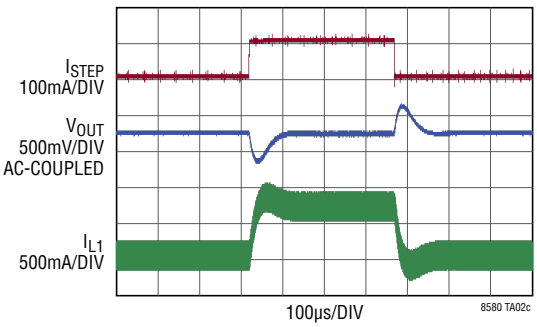


L1: WÜRTH 15µH WE-LQS 74404054150
D1: DIODES INC. SBR1U40LP
C_{IN}: 2.2µF, 35V, 0805, X7R
C_{OUT}: 4.7µF, 16V, 0805, X7R

Efficiency and Power Loss

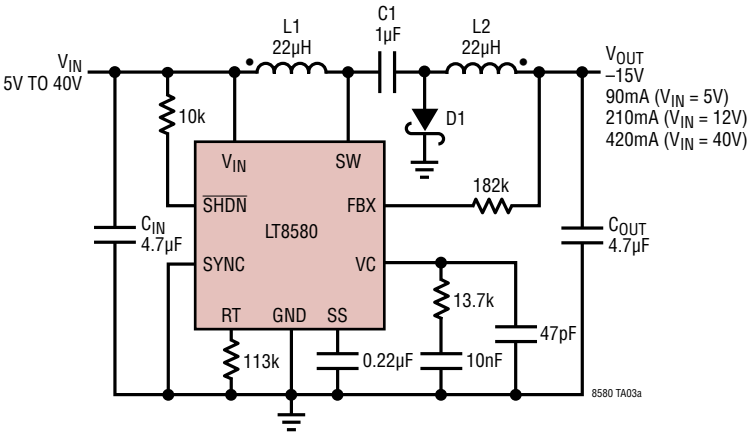


50mA to 150mA to 50mA Output Load Step



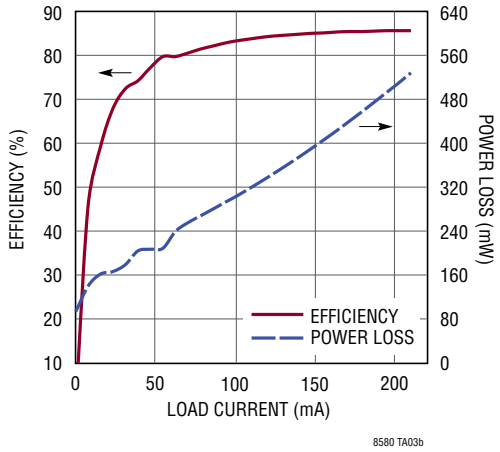
TYPICAL APPLICATIONS

750kHz, –15V Output Inverting Converter Accepts 5V to 40V Input

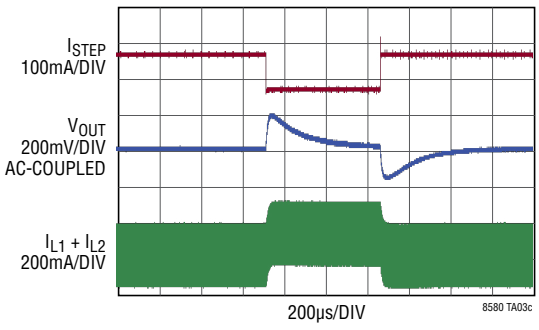


L1, L2: COILCRAFT 22µH MSD7342-223
D1: CENTRAL SEMI CMMSH1-60
C_{IN}: 4.7µF, 50V, 1206, X5R
C_{OUT}: 4.7µF, 25V, 1206, X7R
C1: 1µF, 100V, 0805, X7S

Efficiency and Power Loss (V_{IN} = 12V)

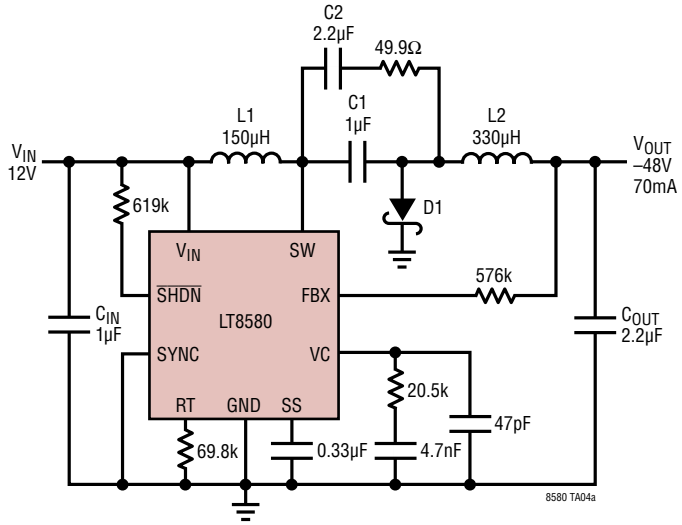


60mA to 160mA to 60mA Output Load Step (V_{IN} = 12V)



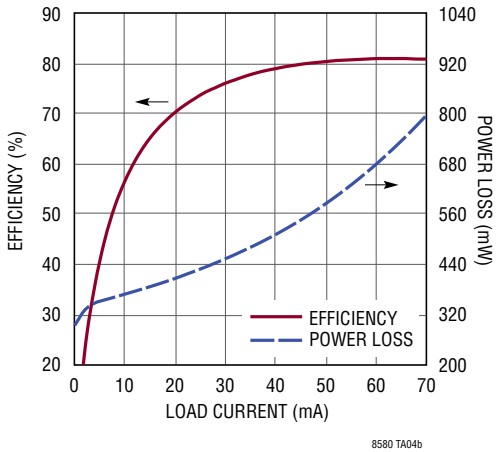
TYPICAL APPLICATIONS

1.2MHz Inverting Converter Generates –48V Output From 12V Input

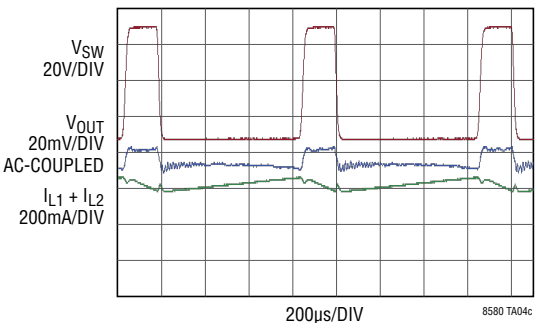


L1: COOPER 150µH DR74-151
L2: COOPER 330µH DR74-331
D1: DIODES, INC. DFLS1100
C_{IN}: 1µF, 50V, 0805, X7R
C_{OUT}: 2.2µF, 100V, 1206, X7R
C1: 1µF, 100V, 0805, X7S
C2: 2.2µF, 100V, 1206, X7S

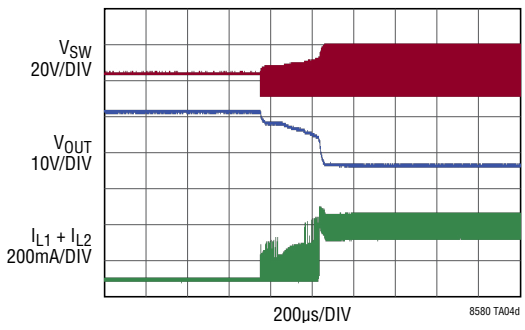
Efficiency and Power Loss



Switching Waveforms



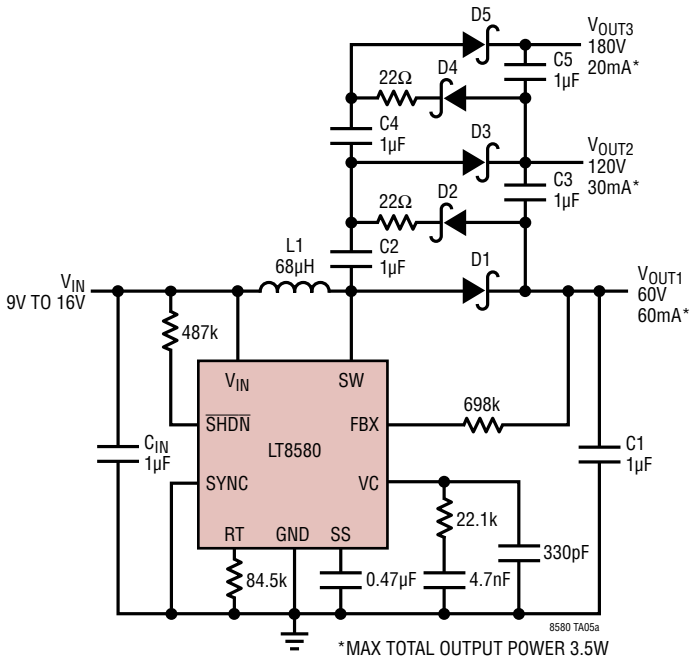
Start-Up Waveforms



TYPICAL APPLICATIONS

VFD (Vacuum Fluorescent Display) Power Supply Switches at 1MHz

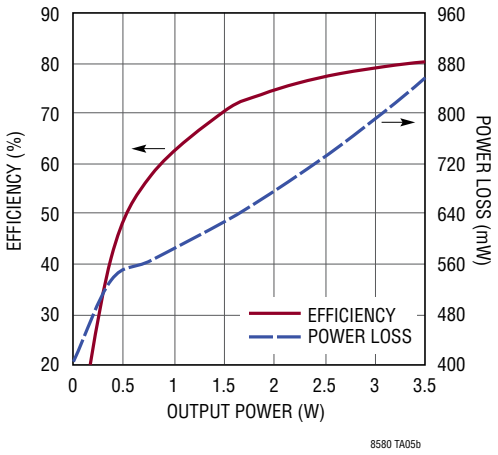
Danger High Voltage! Operation by High Voltage Trained Personnel Only



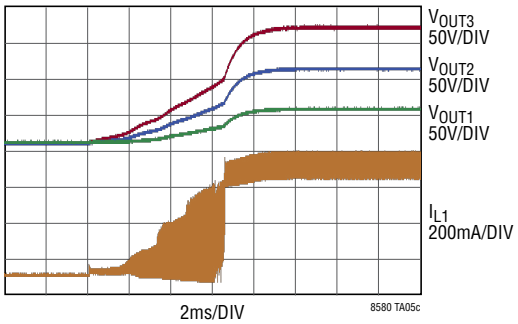
*MAX TOTAL OUTPUT POWER 3.5W

L1: WÜRTH 68µH WE-LQS 74404084680
D1-D5: DIODES, INC. DFLS1100
C_{IN}: 1µF, 100V, 1206, X7R
C1-C5: 1µF, 100V, 1206, X7S

Efficiency and Power Loss (V_{IN} = 12V with Load on V_{OUT3})

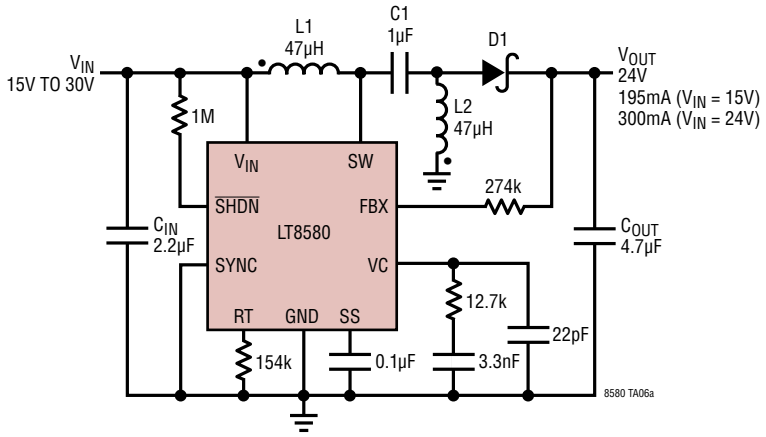


Start-Up Waveforms



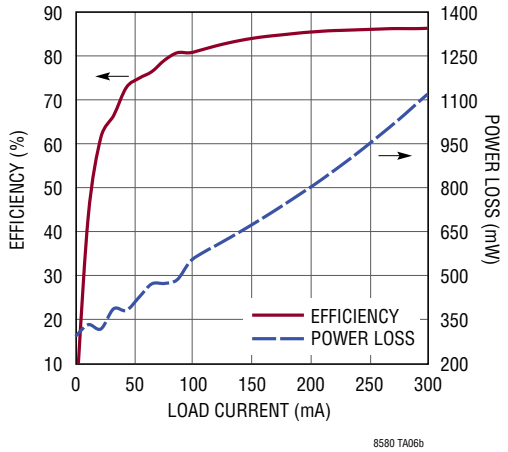
TYPICAL APPLICATIONS

550kHz SEPIC Converter Generates 24V from 15V to 30V Input

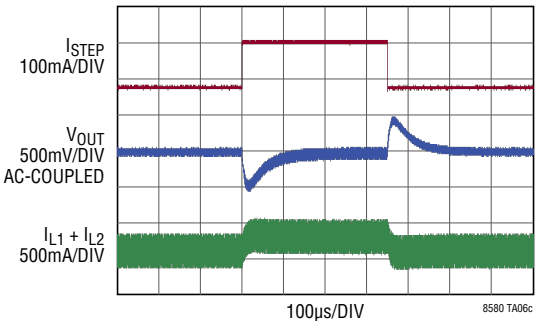


L1, L2: COILCRAFT 47µH MSD7342-473
D1: DIODES INC. DFLS1100
C_{IN}: 2.2µF, 35V, 0805, X7R
C_{OUT}: 4.7µF, 35V, 1206, X7R
C1: 1µF, 100V, 0805, X7S

Efficiency and Power Loss (V_{IN} = 24V)

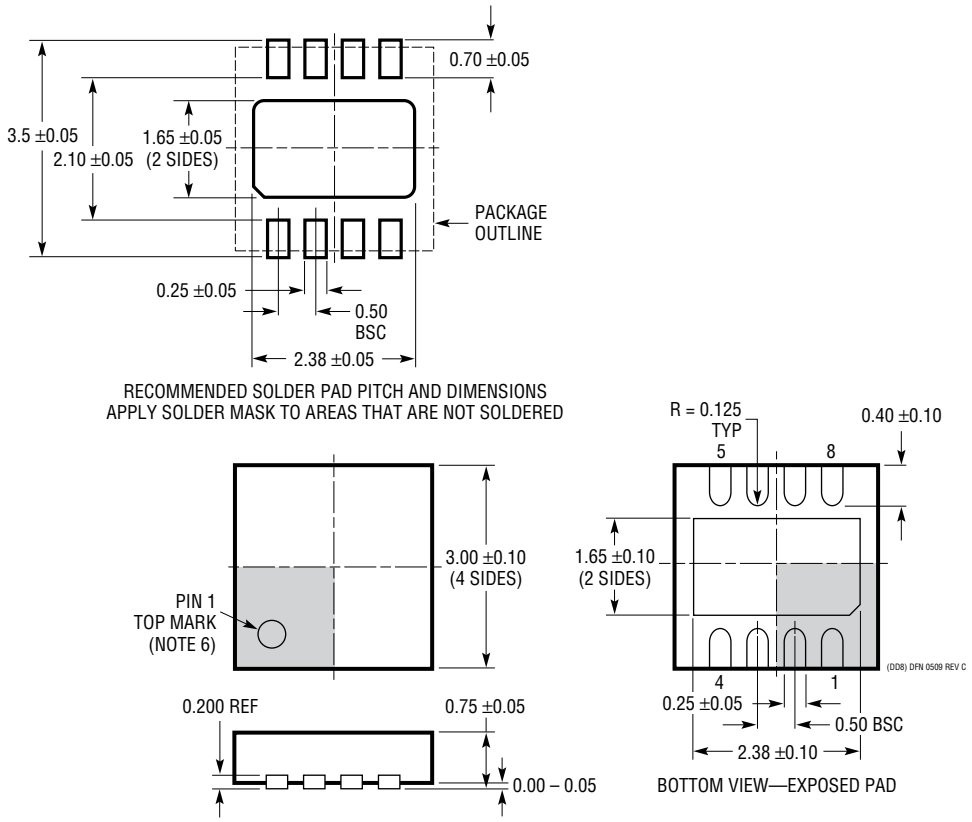


Transient Response with 100mA to 225mA to 100mA Output Load Step (V_{IN} = 24V)



PACKAGE DESCRIPTION

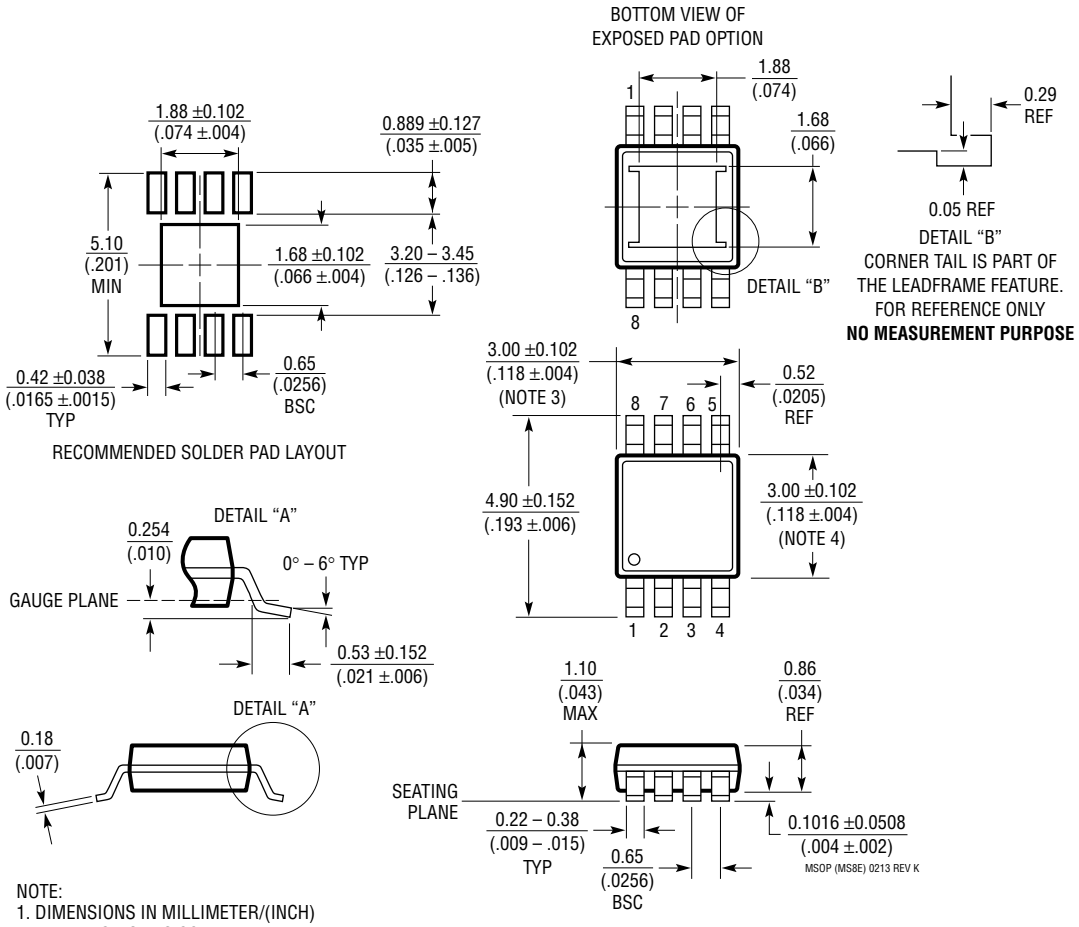
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

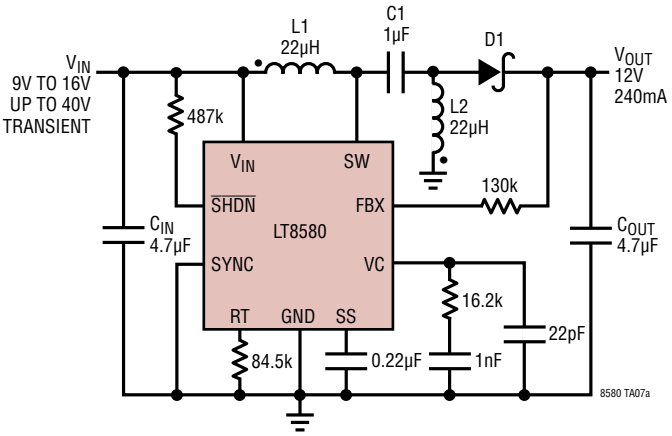
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/16	Changed Minimum On-Time in the Electrical Characteristics table to typical room value instead of worst case.	3
		Added Minimum On-Time vs Temperature graph.	5
		Added text and equations explaining minimum on-time.	9
		Clarified inductor paragraph in the Applications Information section.	10, 11
		Adjusted R_C, R_L, R_O, g_{ma} and resultant gain and phase margin numbers and plot to better reflect applications and the Electrical Characteristics table.	11, 14
		Clarified Thermal Calculations section.	17
		Corrected L_{MIN} equation.	21, 22, 23
		Clarified the Related Parts table.	32
B	11/19	Add AEC-Q100 Qualification in Progress	1
		Add #W Part Numbers	2

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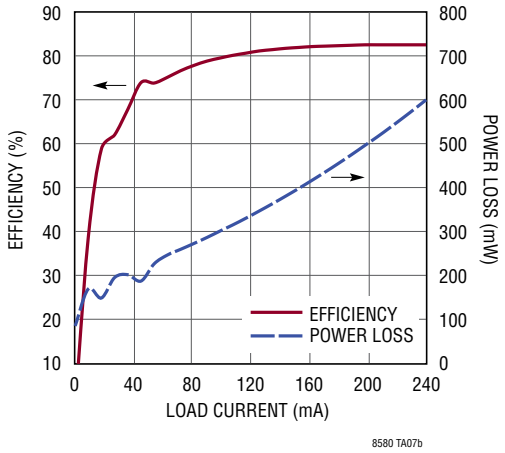
TYPICAL APPLICATION

12V Battery Stabilizer Survives 40V Transients



L1, L2: WÜRTH 22µH WE-DD 744877220
D1: DIODES INC. DFLS1100
C_{IN}: 4.7µF, 50V, 1206, X7R
C_{OUT}: 4.7µF, 25V, 1206, X7R
C1: 1µF, 100V, 0805, X7S

Efficiency and Power Loss (V_{IN} = 12V)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1613	550mA (I_{SW}), 1.4MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 0.9V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT1618	1.5A (I_{SW}), 1.4MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$ = 35V, I_Q = 1.8mA, I_{SD} < 1µA, MS10, 3mm × 3mm DFN Packages
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1935	2A (I_{SW}), 40V, 1.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.3V to 16V, $V_{OUT(MAX)}$ = 38V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT1944/LT1944-1	Dual Output 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, MS10 Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, MS8E Package
LT3467	1.1A (I_{SW}), 1.3MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} < 1µA, ThinSOT, 2mm × 3mm DFN Packages
LT3477	42V, 3A, 3.5MHz Boost, Buck-Boost, Buck LED Driver	V_{IN}: 2.5V to 25V, $V_{OUT(MAX)}$ = 40V, Analog/PWM, I_{SD} < 1µA, QFN, TSSOP-20E Packages
LT3479	3A Full-Featured DC/DC Converter with Soft-Start and Inrush Current Protection	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 40V, I_Q = 5mA, I_{SD} < 1µA, DFN, TSSOP Packages
LT3580	2A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 32V, $V_{OUT(MAX)}$ = 42V, I_Q = 1mA, I_{SD} = <1µA, 3mm × 3mm DFN-8, MSOP-8E
LT3581	3.3A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 22V, $V_{OUT(MAX)}$ = 42V, I_Q = 1.9mA, I_{SD} = <1µA, 4mm × 3mm DFN-14, MSOP-16E
LT3579	6A (I_{SW}), 42V, 2.5MHz, High Efficiency, Step-Up DC/DC Converter	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 42V, I_Q = 1.9mA, I_{SD} = <1µA, 4mm × 5mm QFN-20, TSSOP-20
LT8582	Dual Channel, 3A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 22V, $V_{OUT(MAX)}$ = 42V, I_Q = 2.1mA, I_{SD} = <1µA, 4mm × 7mm DFN-24

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