SNx414 and SNx4LS14 Hex Schmitt-Trigger Inverters

1 Features

- Operation From Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

2 Applications

- HVAC Gateways
- Residential Ductless Air Conditioning Outdoor Units
- Robotic Controls
- Industrial Stepper Motors
- Power Meter and Power Analyzers
- Digital Input Modules for Factory Automation

3 Description

Each circuit in SNx414 and SNx4LS14 functions as an inverter. However, because of the Schmitt-Trigger action, they have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

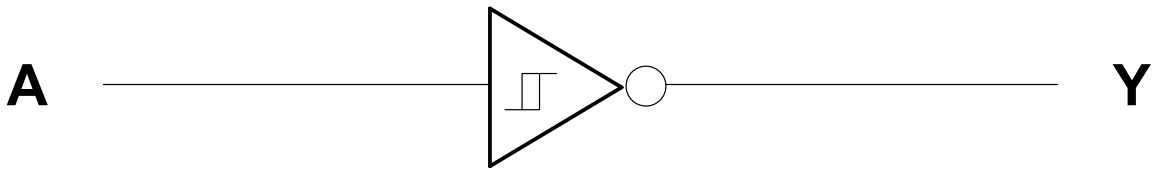
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN7414, SN74LS14	SOIC (14)	4.90 mm × 3.91 mm
	SSOP (14)	6.20 mm × 5.30 mm
	PDIP (14)	19.30 mm × 6.35 mm
	SO (14)	10.30 mm × 5.30 mm
SN5414, SN54LS14	CDIP (14)	19.56 mm × 6.67 mm
	CFP (14)	9.21 mm × 5.97 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

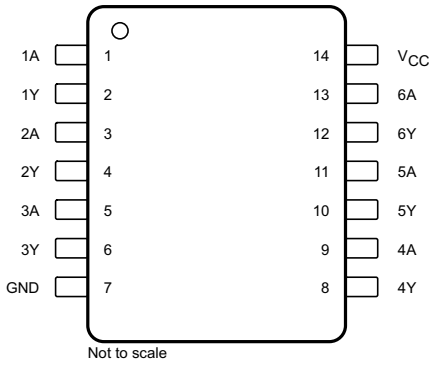
Changes from Revision B (February 2002) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table; see the *Package Option Addendum* at the end of the data sheet ... 1
- Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information* table From: 86°C/W To: 90.1°C/W (D), From: 96°C/W To: 105.4°C/W (DB), From: 80°C/W To: 54.9°C/W (N), and From: 76°C/W To: 88.8°C/W (NS) ... 4

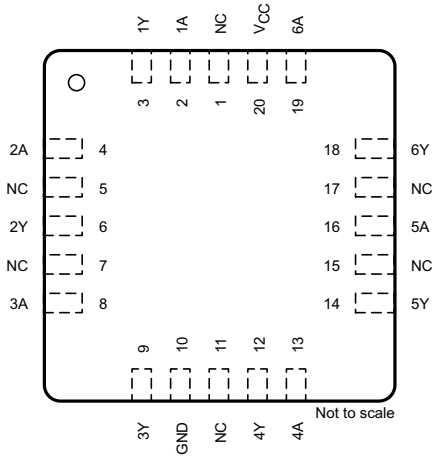
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5 Pin Configuration and Functions

D, DB, N, NS, J, or W Package
14-Pin SOIC, SSOP, PDIP, SO, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, CDIP, PDIP,TSSOP, CFP	LCCC		
1A	1	2	I	Channel 1 input
1Y	2	3	O	Channel 1 output
2A	3	4	I	Channel 2 input
2Y	4	6	O	Channel 2 output
3A	5	8	I	Channel 3 input
3Y	6	9	O	Channel 3 output
4A	9	13	I	Channel 4 input
4Y	8	12	O	Channel 4 output
5A	11	16	I	Channel 5 input
5Y	10	14	O	Channel 5 output
6A	13	19	I	Channel 6 input
6Y	12	18	O	Channel 6 output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V_{CC}	14	20	—	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage	SNx414		5.5	V
	SNx4LS14		7	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN5414, SN54LS14	4.5	5	5.5	V
		SN7414, SN74LS14	4.75	5	5.25	
I_{OH}	High-level output current	SN5414, SN7414			–0.8	mA
		SN54LS14, SN74LS14			–0.4	
I_{OL}	Low-level output current	SN5414, SN7414			16	mA
		SN54LS14			4	
		SN74LS14			8	
T_A	Operating free-air temperature	SN5414, SN54LS14	–55		125	°C
		SN7414, SN74LS14	0		70	

6.4 Thermal Information

THERMAL METRIC(1)		SNx414, SNx4LS14				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	90.1	105.4	54.9	88.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	57.3	42.5	46.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.3	52.7	34.7	47.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.9	22.5	27.8	16.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.1	52.2	34.6	47.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package termal impedance is calculated in accordance with JESD 51-7.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{T+}	V_{CC} = 5 V	SNx414	1.5	1.7	2	V
		SNx4LS14	1.4	1.6	1.9	
V_{T-}	V_{CC} = 5 V	SNx414	0.6	0.9	1.1	V
		SNx4LS14	0.5	0.8	1	
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V		0.4	0.8		V
V_{IK}	V_{CC} = MIN, I_I = –12 mA, SNx414				–1.5	V
	V_{CC} = MIN, I_I = –18 mA, SNx4LS14				–1.5	
V_{OH}	V_{CC} = MIN, V_I = 0.6 V, I_{OH} = –0.8 mA, SNx414		2.4	3.4		V
	V_{CC} = MIN, V_I = 0.5 V, I_{OH} = –0.4 mA, SNx4LS14		2.4	3.4		
V_{OL}	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA, SNx414			0.2	0.4	V
	V_{CC} = MIN, V_I = 1.9 V	I_{OL} = 4 mA, SNx4LS14		0.25	0.4	
		I_{OL} = 8 mA, SN74LS14		0.35	0.5	
I_{T+}	V_{CC} = 5 V, V_I = V_{T+}	SNx414		–0.43		mA
		SNx4LS14		–0.14		
I_{T-}	V_{CC} = 5 V, V_I = V_{T-}	SNx414		–0.56		mA
		SNx4LS14		–0.18		
I_I	V_{CC} = MAX, V_I = 5.5 V, SNx414				1	mA
	V_{CC} = MAX, V_I = 7 V, SNx4LS14				0.1	
I_{IH}	V_{CC} = MAX, V_{IH} = 2.4 V, SNx414				40	μA
	V_{CC} = MAX, V_{IH} = 2.7 V, SNx4LS14				20	
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V	SNx414		–0.8	–1.2	mA
		SNx4LS14			–0.4	
I_{OS}[3]	V_{CC} = MAX	SNx414	–18		–55	mA
		SNx4LS14	–20		–100	
I_{CCH}	V_{CC} = MAX	SNx414		22	36	mA
		SNx4LS14		8.6	16	
I_{CCL}	V_{CC} = MAX	SNx414		39	60	mA
		SNx4LS14		12	21	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) Not more than one output should be shorted at a time.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted; see Figure 20)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω and C_L = 15 pF, or R_L = 2 kΩ and C_L = 15 pF		15	22	ns
t_{PHL}	A	Y	R_L = 400 Ω and C_L = 15 pF, or R_L = 2 kΩ and C_L = 15 pF		15	22	ns

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6.7 Typical Characteristics

6.7.1 SNx414 Circuits

Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for SN5414 only.

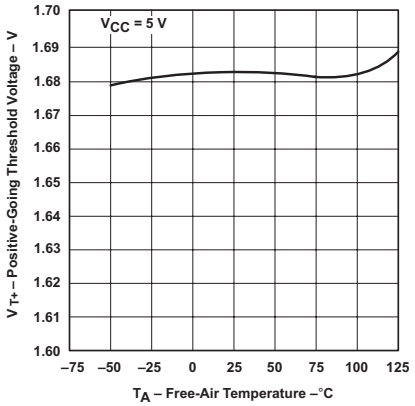


Figure 1. Positive-Going Threshold Voltage vs Free-Air Temperature

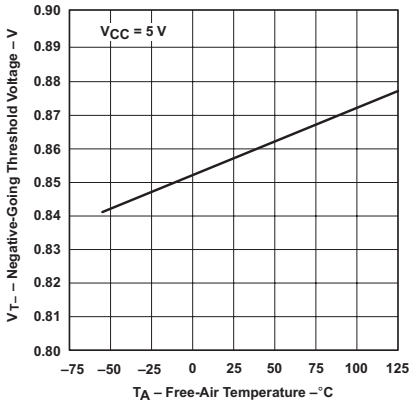


Figure 2. Negative-Going Threshold Voltage vs Free-Air Temperature

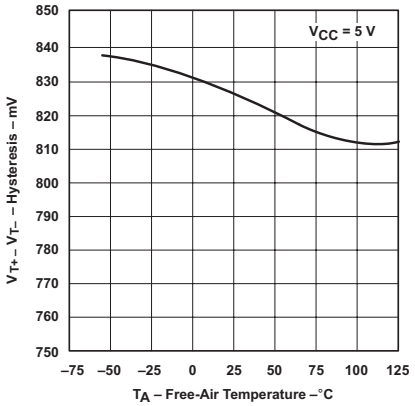


Figure 3. Hysteresis vs Free-Air Temperature

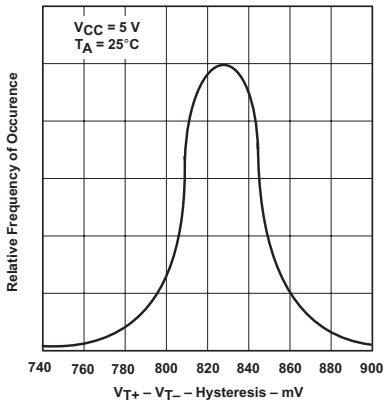


Figure 4. Distribution of Units for Hysteresis

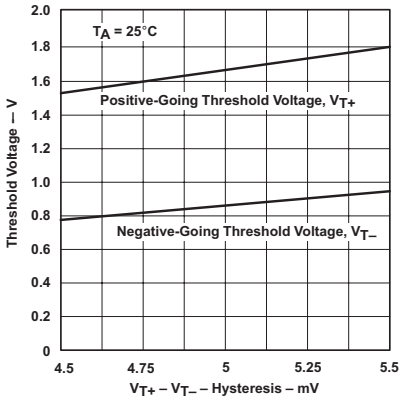


Figure 5. Threshold Voltages vs Supply Voltage

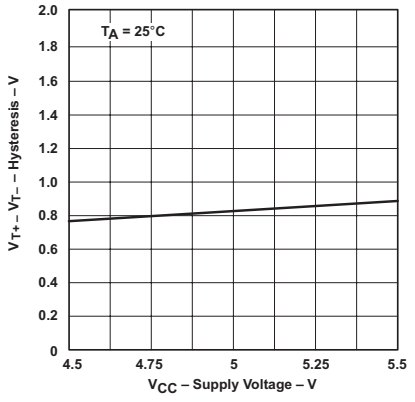


Figure 6. Hysteresis vs Supply Voltage

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SNx414 Circuits (continued)

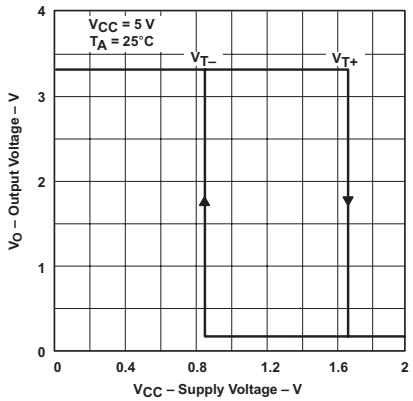


Figure 7. Output Voltage vs Input Voltage

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6.7.2 SNx4LS14 Circuits

Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for SNx4LS14 only.

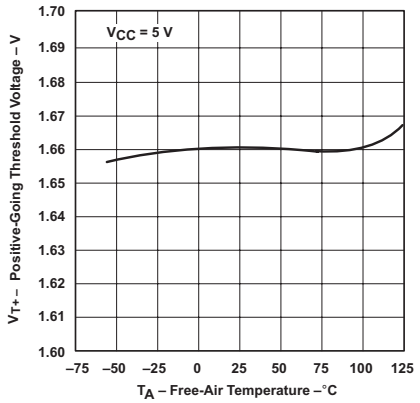


Figure 8. Positive-Going Threshold Voltage vs Free-Air Temperature

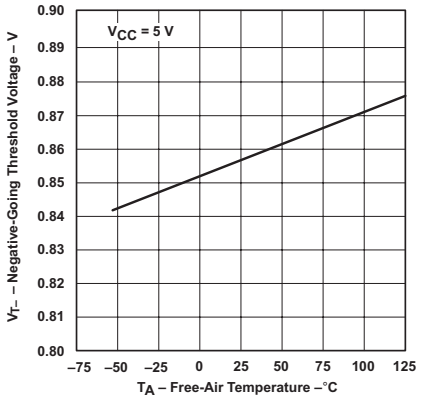


Figure 9. Negative-Going Threshold Voltage vs Free-Air Temperature

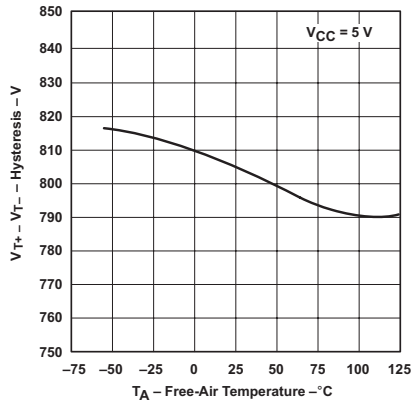


Figure 10. Hysteresis vs Free-Air Temperature

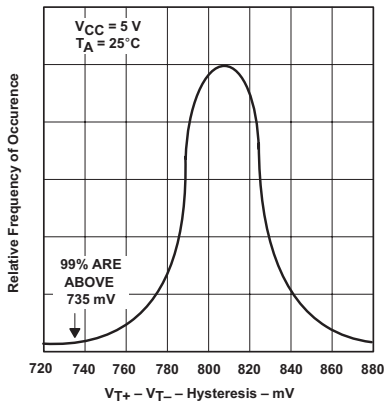


Figure 11. Distribution of Units for Hysteresis

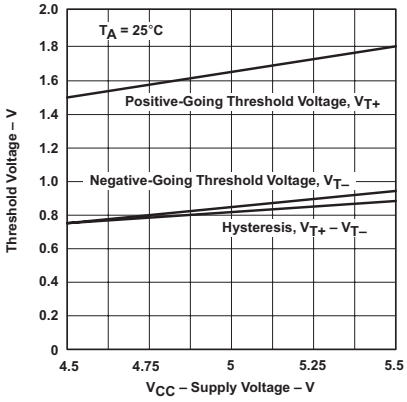


Figure 12. Threshold Voltages and Hysteresis vs Supply Voltage

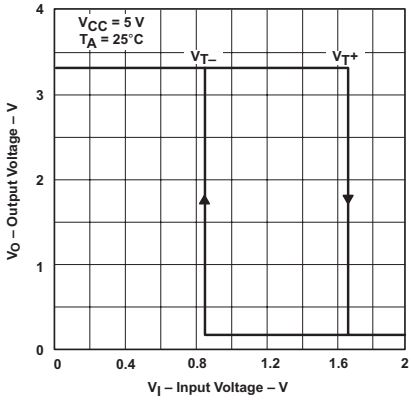


Figure 13. Output Voltage vs Input Voltage

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7 Parameter Measurement Information

7.1 Series SN5414 and SN7414 Devices

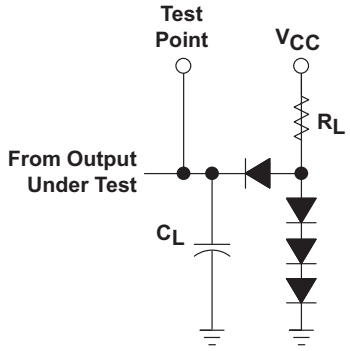


Figure 14. Load Circuit For 2-State Totem-Pole Outputs

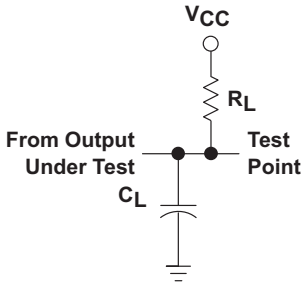


Figure 15. Load Circuit For Open-Collector Outputs

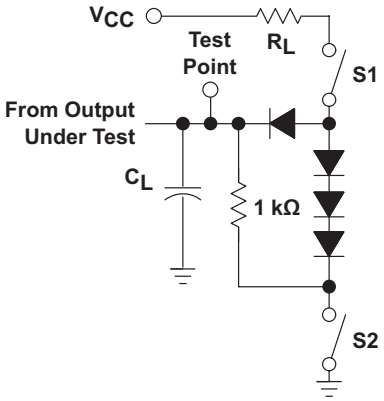


Figure 16. Load Circuit For 3-State Outputs

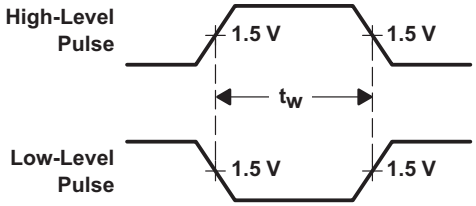


Figure 17. Voltage Waveforms Pulse Durations

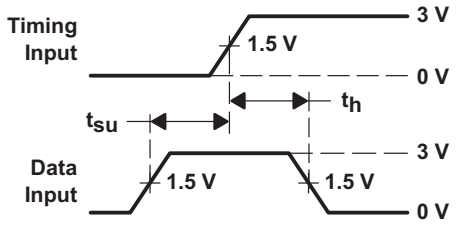


Figure 18. Voltage Waveforms Setup and Hold Times

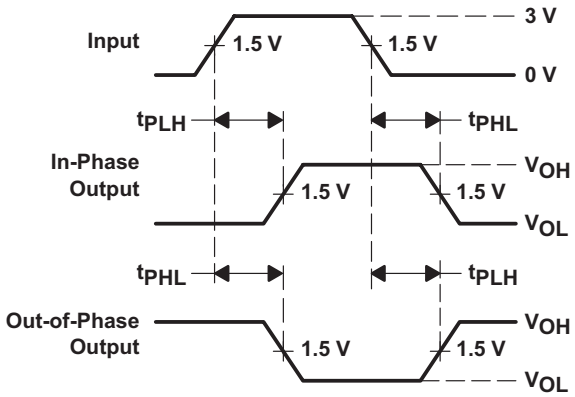
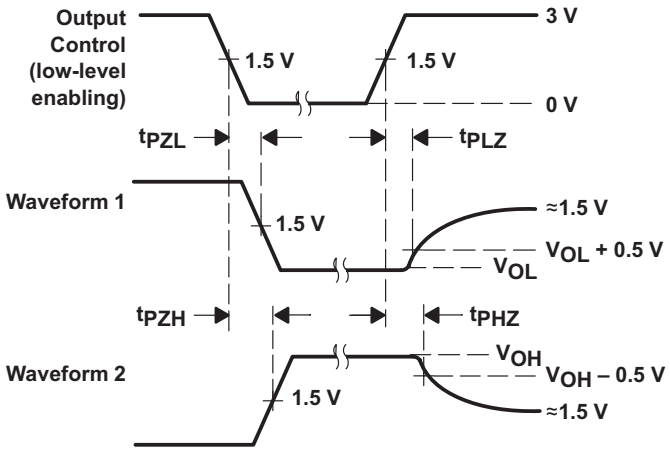


Figure 19. Voltage Waveforms Propagation Delay Times

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Series SN5414 and SN7414 Devices (continued)



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series SN5414 and SN7414 devices and t_r and $t_f \leq 2.5$ ns for Series SN54S14 and SN74S14 devices.

F. The outputs are measured one at a time with one input transition per measurement.

Figure 20. Voltage Waveforms Enable and Disable Times, 3-State Outputs

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7.2 Series SN54LS14 and SN74LS14 Devices

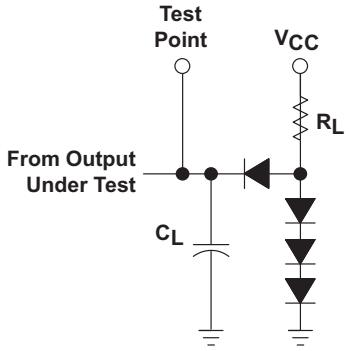


Figure 21. Load Circuit For 2-State Totem-Pole Outputs

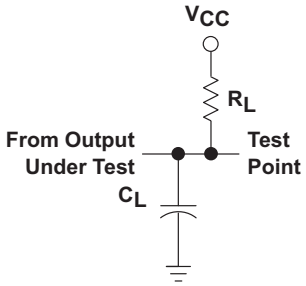


Figure 22. Load Circuit For Open-Collector Outputs

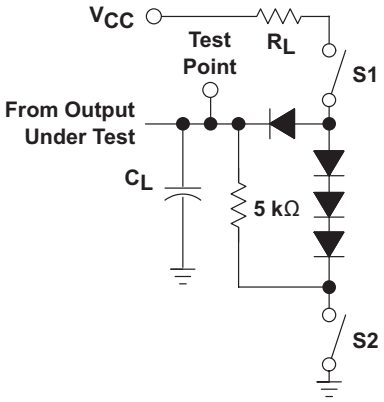


Figure 23. Load Circuit For 3-State Outputs

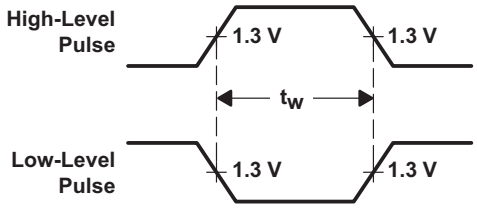


Figure 24. Voltage Waveforms Pulse Durations

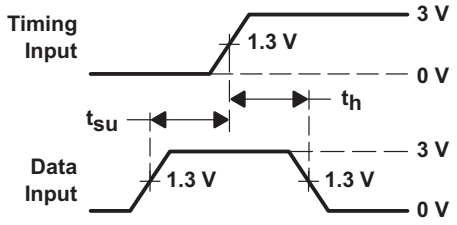


Figure 25. Voltage Waveforms Setup and Hold Times

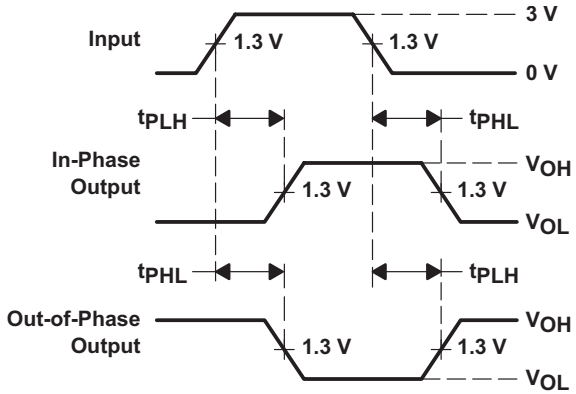
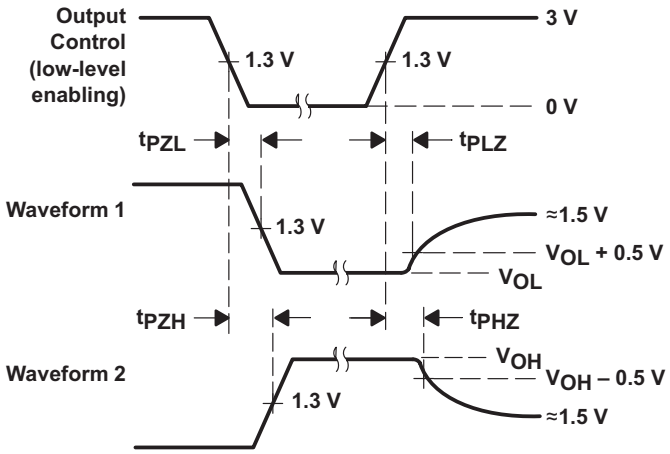


Figure 26. Voltage Waveforms Propagation Delay Times

Series SN54LS14 and SN74LS14 Devices (continued)



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.

G. The outputs are measured one at a time with one input transition per measurement.

Figure 27. Voltage Waveforms Enable and Disable Times, 3-State Outputs

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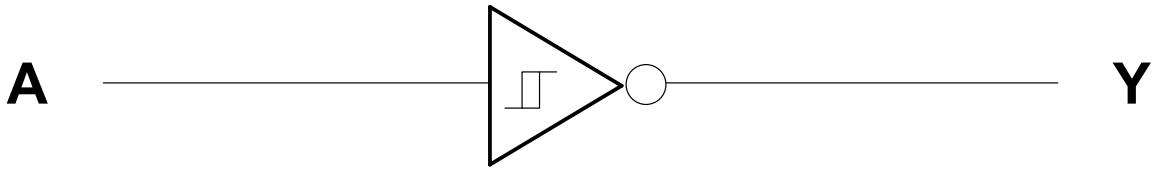
8 Detailed Description

8.1 Overview

The SNx414 and SNx4LS14 Schmitt-Trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

Schmitt-Trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs.

8.2 Functional Block Diagram



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8.3 Feature Description

The device can operate from very slow transition edge inputs. This device has high noise immunity.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx414 and SNx4LS14.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

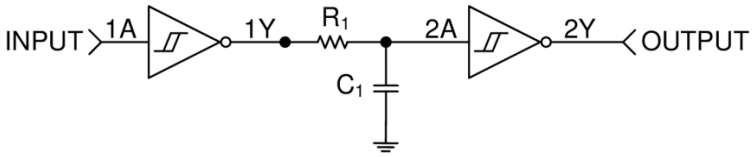
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx414 and SNx4LS14 device is a Schmitt-Trigger input CMOS device that can be used for a multitude of inverting buffer type functions. The application shown here takes advantage of the Schmitt-Trigger inputs to produce a delay for a logic input.

9.2 Typical Application



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Figure 28. Simplified Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

This circuit is designed around an RC network that produces a slow input to the second inverter. The RC time constant (τ) is calculated from: $\tau = RC$.

The delay time for this circuit is from $t_{delay(min)} = -\ln |1 - V_{T+(min)} / V_{CC}| \tau$ to $t_{delay(max)} = -\ln |1 - V_{T+(max)} / V_{CC}| \tau$. It must be noted that the delay is consistent for each device, but because the switching threshold is only ensured between the minimum and maximum value, the output pulse length varies between devices. These values must be calculated by using the minimum and maximum ensured V_{T+} values in the *Electrical Characteristics*.

The resistor value must be chosen such that the maximum current to and from the SNx414/SNx4LS14 is 8 mA at 5-V V_{CC}.

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Typical Application (continued)

9.2.3 Application Curve

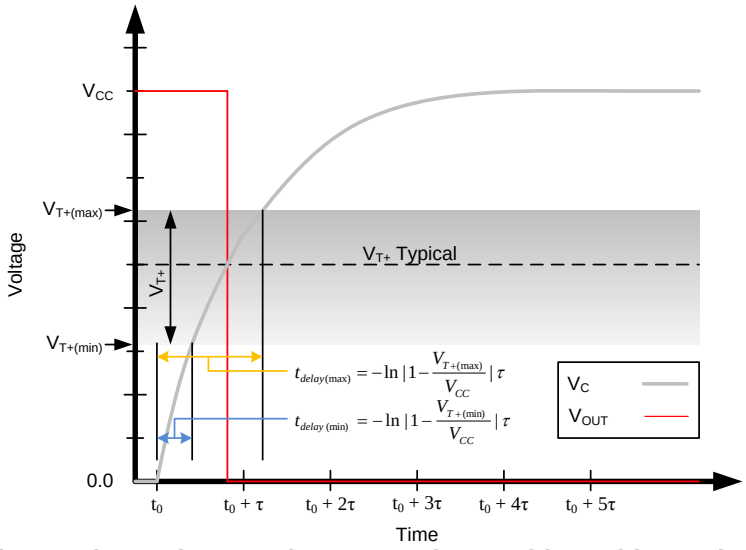


Figure 29. Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold

9.3 System Examples

Here are some examples of various applications using the SNx414 and SNx4LS14 device.

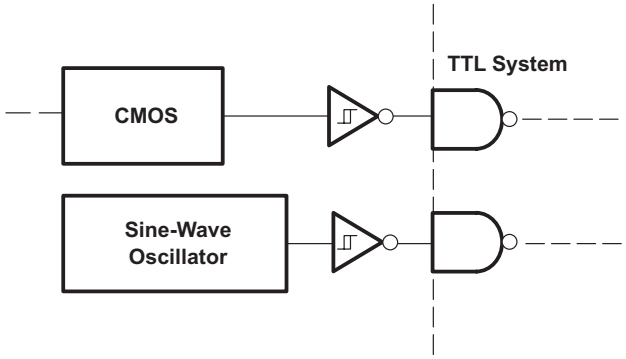


Figure 30. TTL System Interface For Slow Input Waveforms

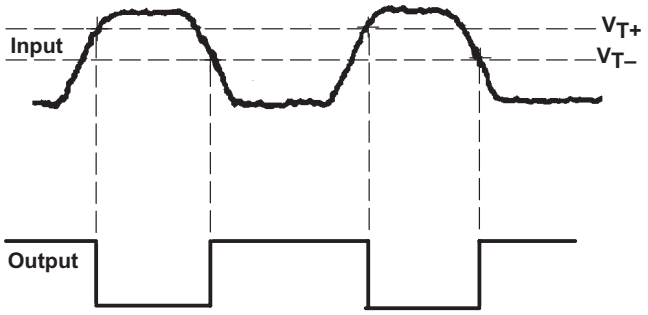


Figure 31. Pulse Shaper

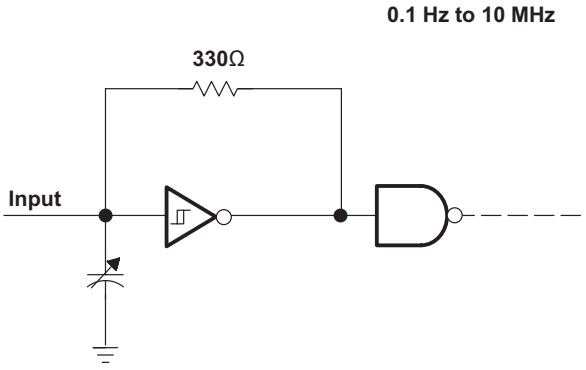


Figure 32. Multivibrator

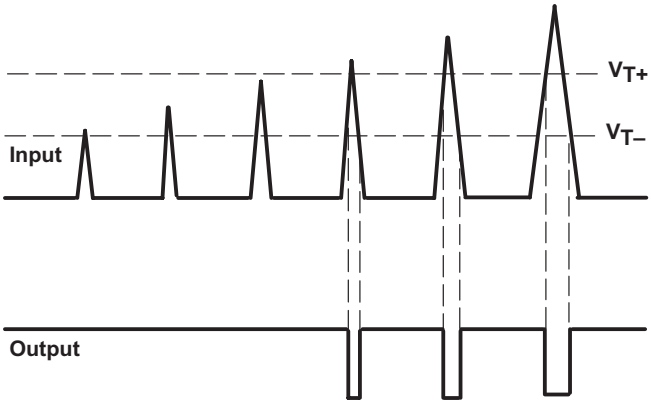
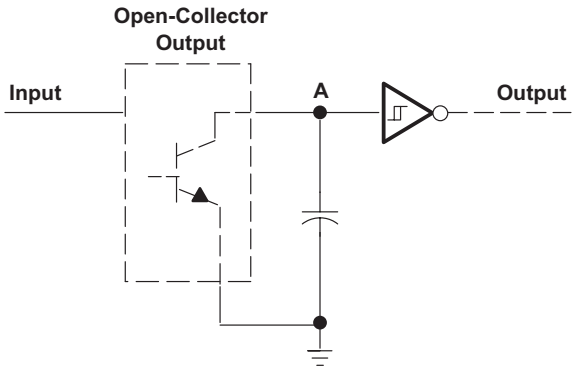


Figure 33. Threshold Detector



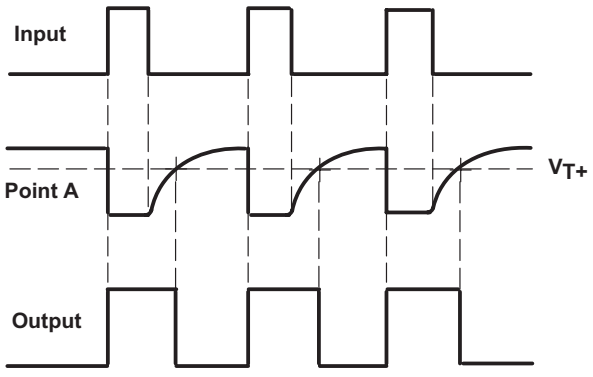


Figure 34. Pulse Stretcher

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10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. The V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends using a 0.1-µF capacitor on the V_{CC} terminal, and must be placed as close as possible to the pin for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

11.2 Layout Example

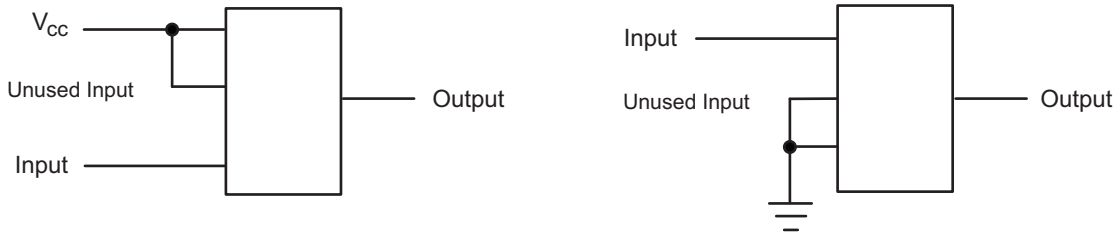


Figure 35. Layout Diagram

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12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN5414	Click here	Click here	Click here	Click here	Click here
SN54LS14	Click here	Click here	Click here	Click here	Click here
SN7414	Click here	Click here	Click here	Click here	Click here
SN74LS14	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9665801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9665801Q2A SNJ54LS 14FK	Samples
5962-9665801QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9665801QCA SNJ54LS14J	Samples
5962-9665801QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9665801QDA SNJ54LS14W	Samples
5962-9665801VDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9665801VDA SNV54LS14W	Samples
JM38510/31302BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31302BCA	Samples
M38510/31302BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31302BCA	Samples
SN5414J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN5414J	Samples
SN54LS14J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54LS14J	Samples
SN7414D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	7414	Samples
SN7414DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	7414	Samples
SN7414DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	7414	Samples
SN7414N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN7414N	Samples
SN7414NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN7414	Samples
SN74LS14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS14N	Samples
SN74LS14NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS14N	Samples
SN74LS14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS14	Samples
SNJ5414J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5414J	Samples
SNJ5414W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5414W	Samples
SNJ54LS14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9665801Q2A SNJ54LS 14FK	Samples
SNJ54LS14J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9665801QC A SNJ54LS14J	Samples
SNJ54LS14W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9665801QD A SNJ54LS14W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN5414, SN54LS14, SN54LS14-SP, SN7414, SN74LS14 :

- Catalog: SN7414, SN74LS14, SN54LS14
- Military: SN5414, SN54LS14
- Space: SN54LS14-SP

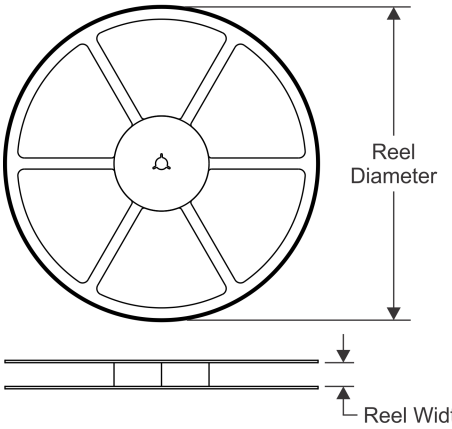
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

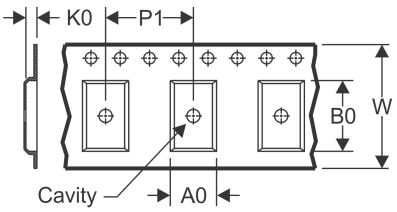
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

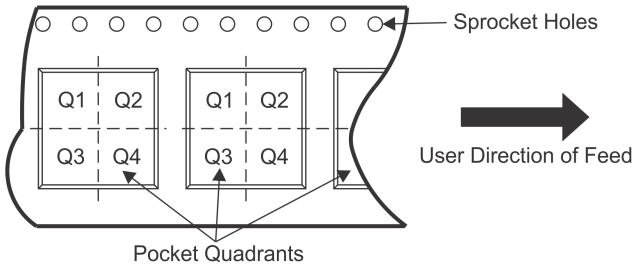


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

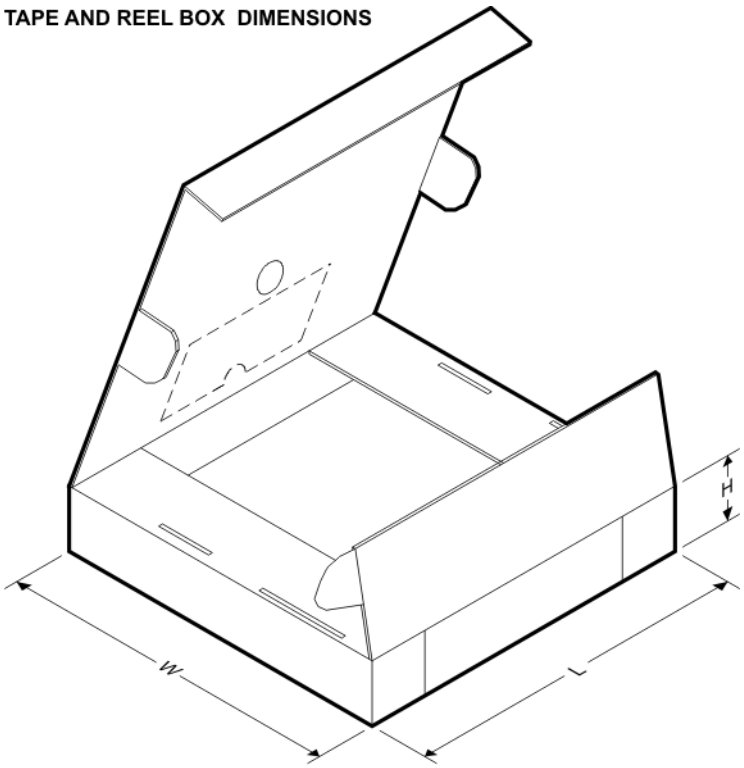
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7414DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN7414NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

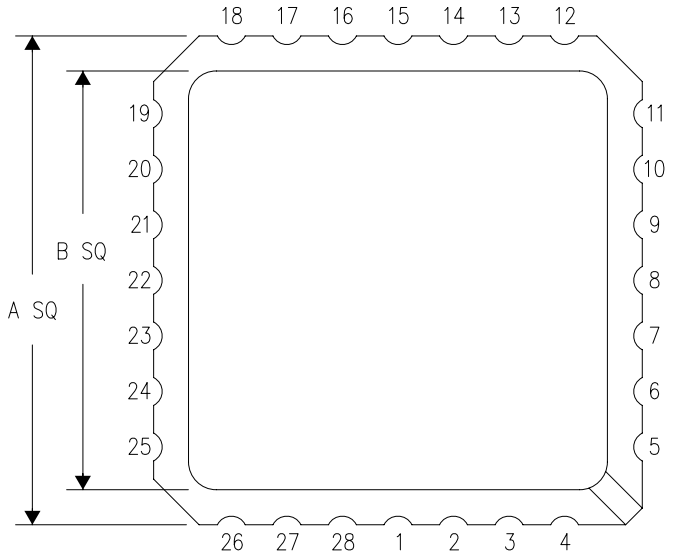


*All dimensions are nominal

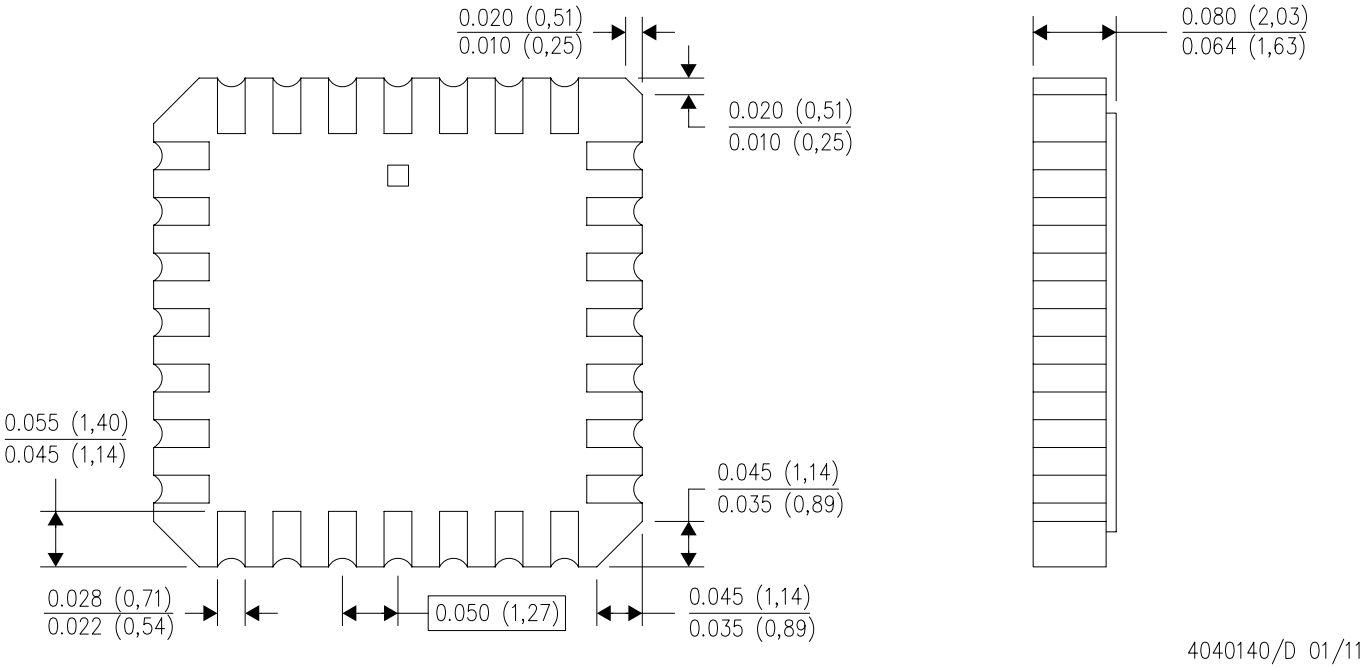
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7414DR	SOIC	D	14	2500	367.0	367.0	38.0
SN7414NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LS14DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS14NSR	SO	NS	14	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



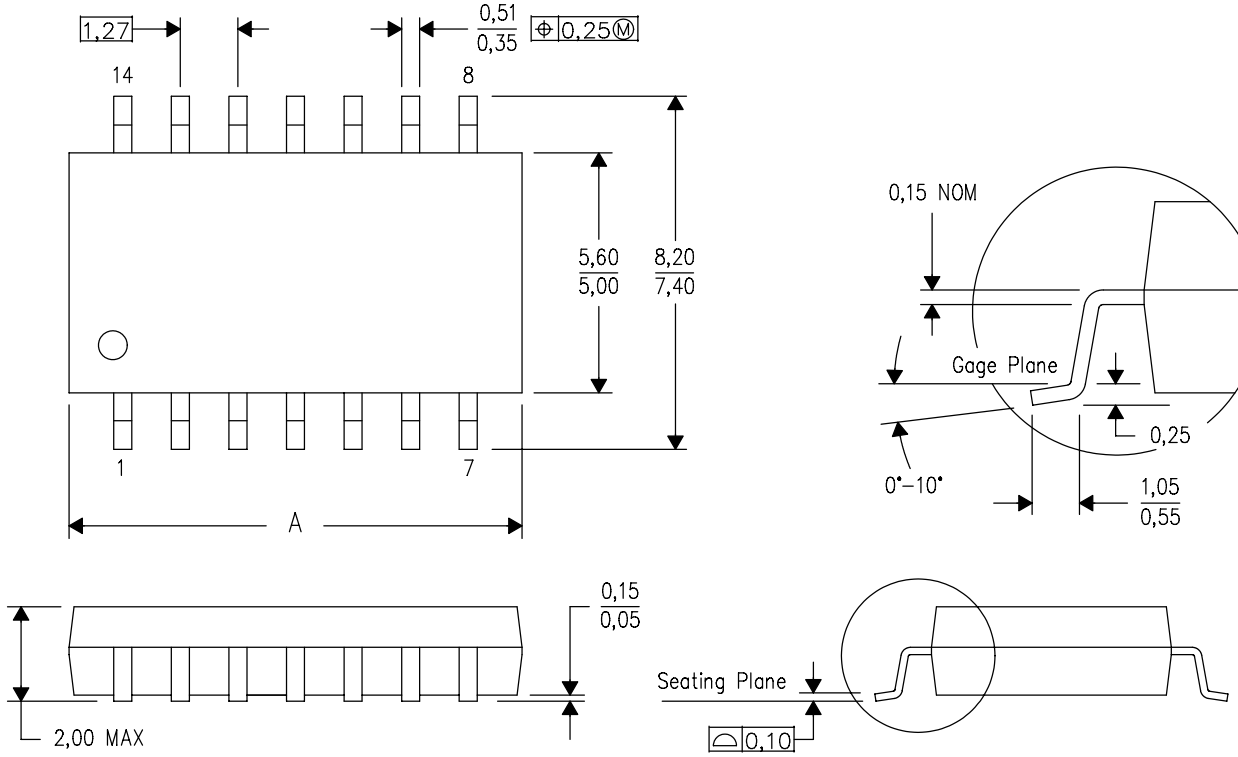
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

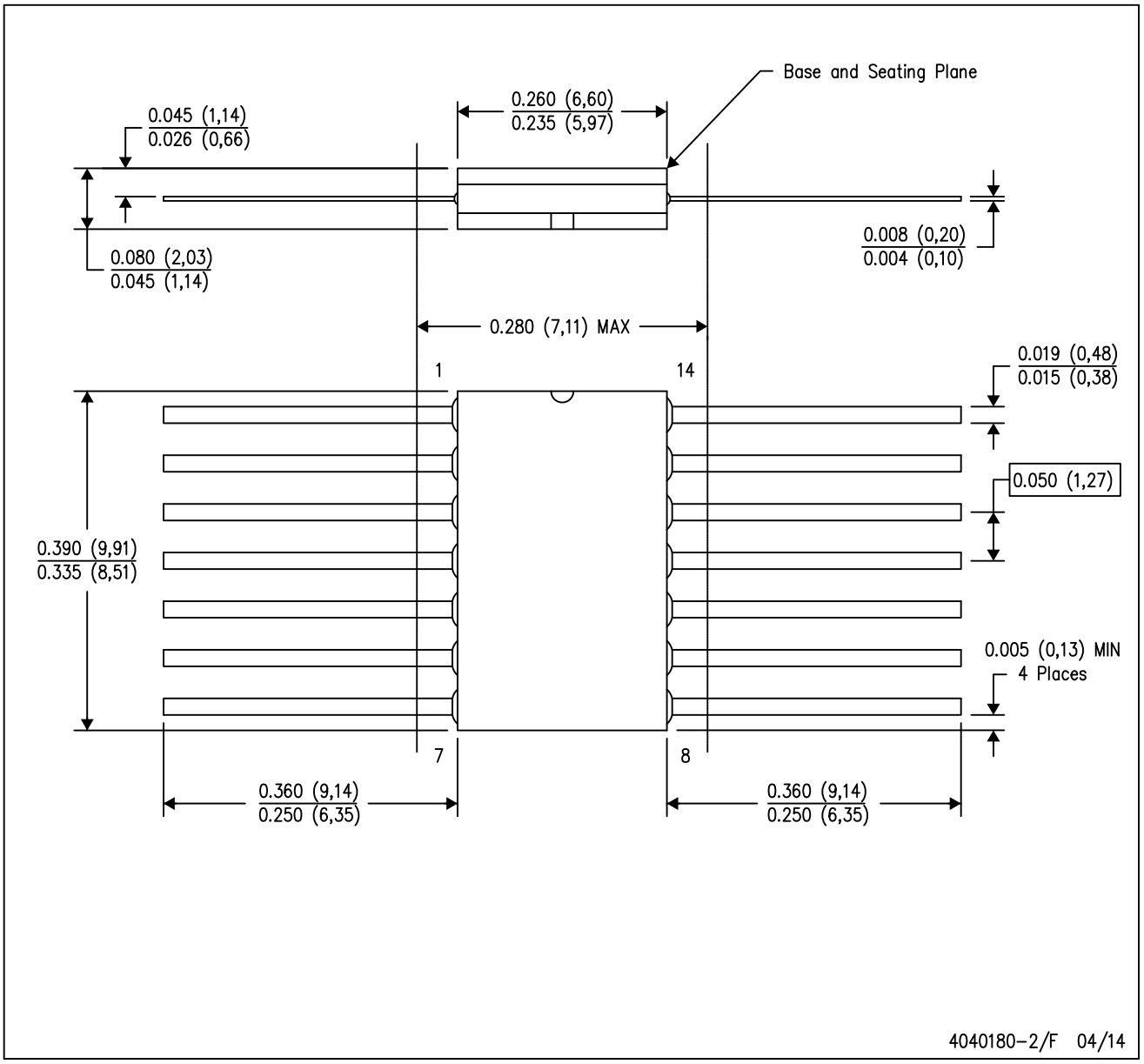


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

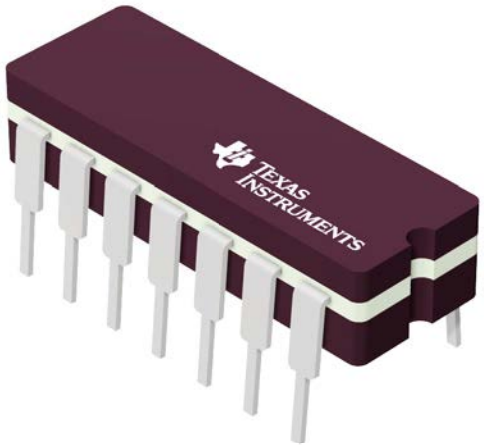


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

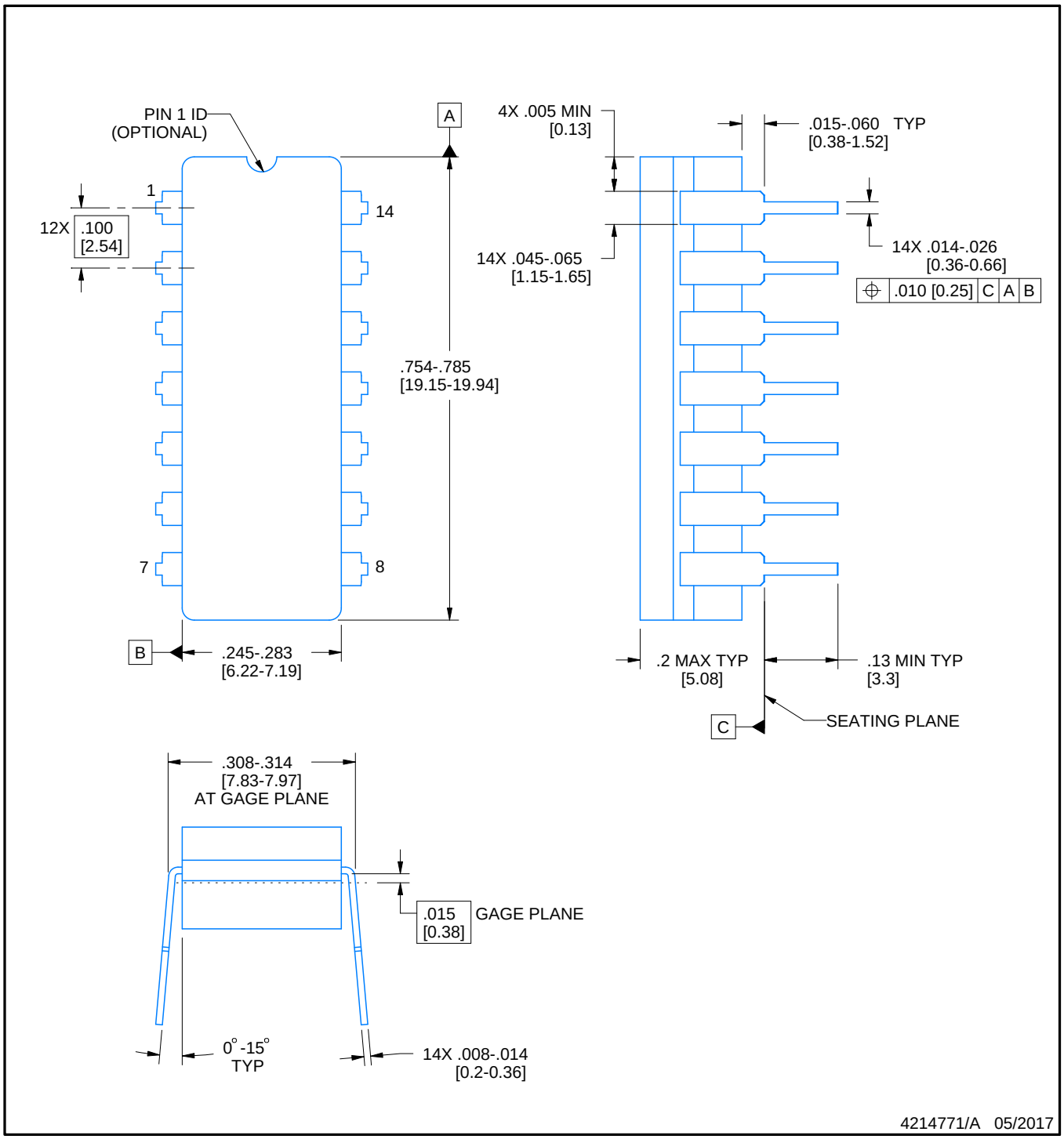


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

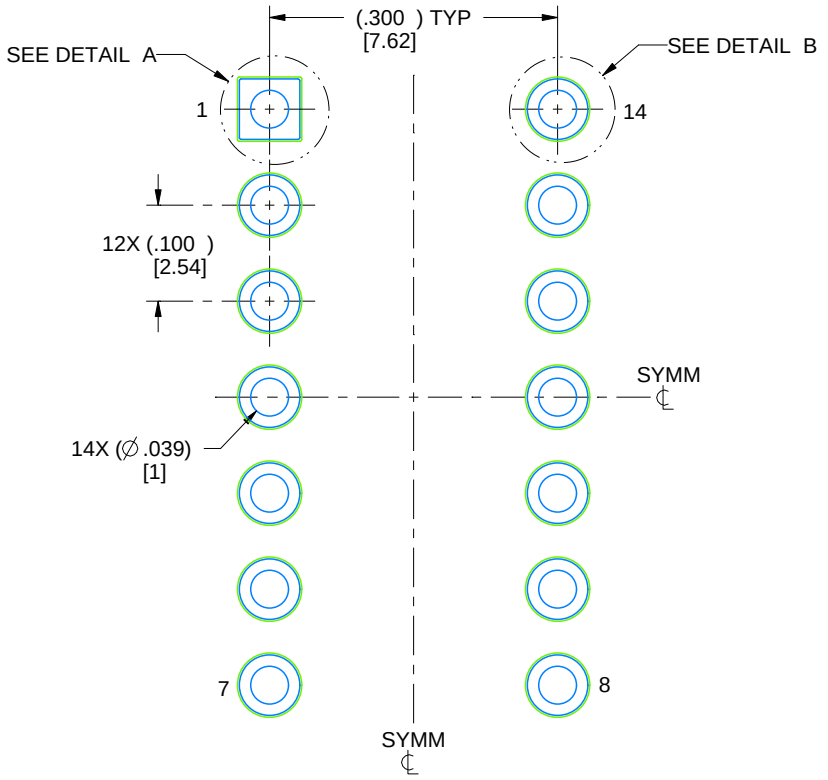
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

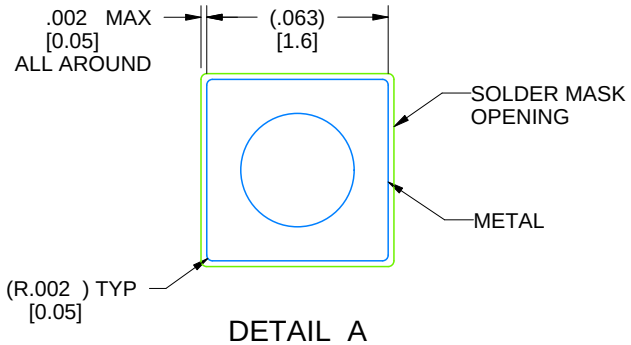
J0014A

CDIP - 5.08 mm max height

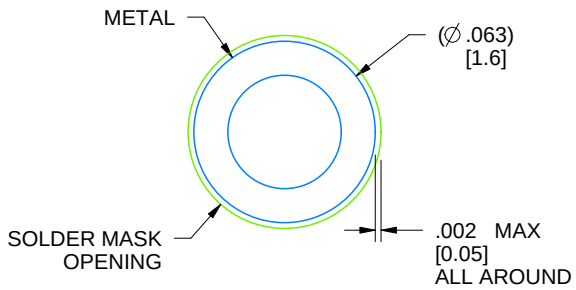
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



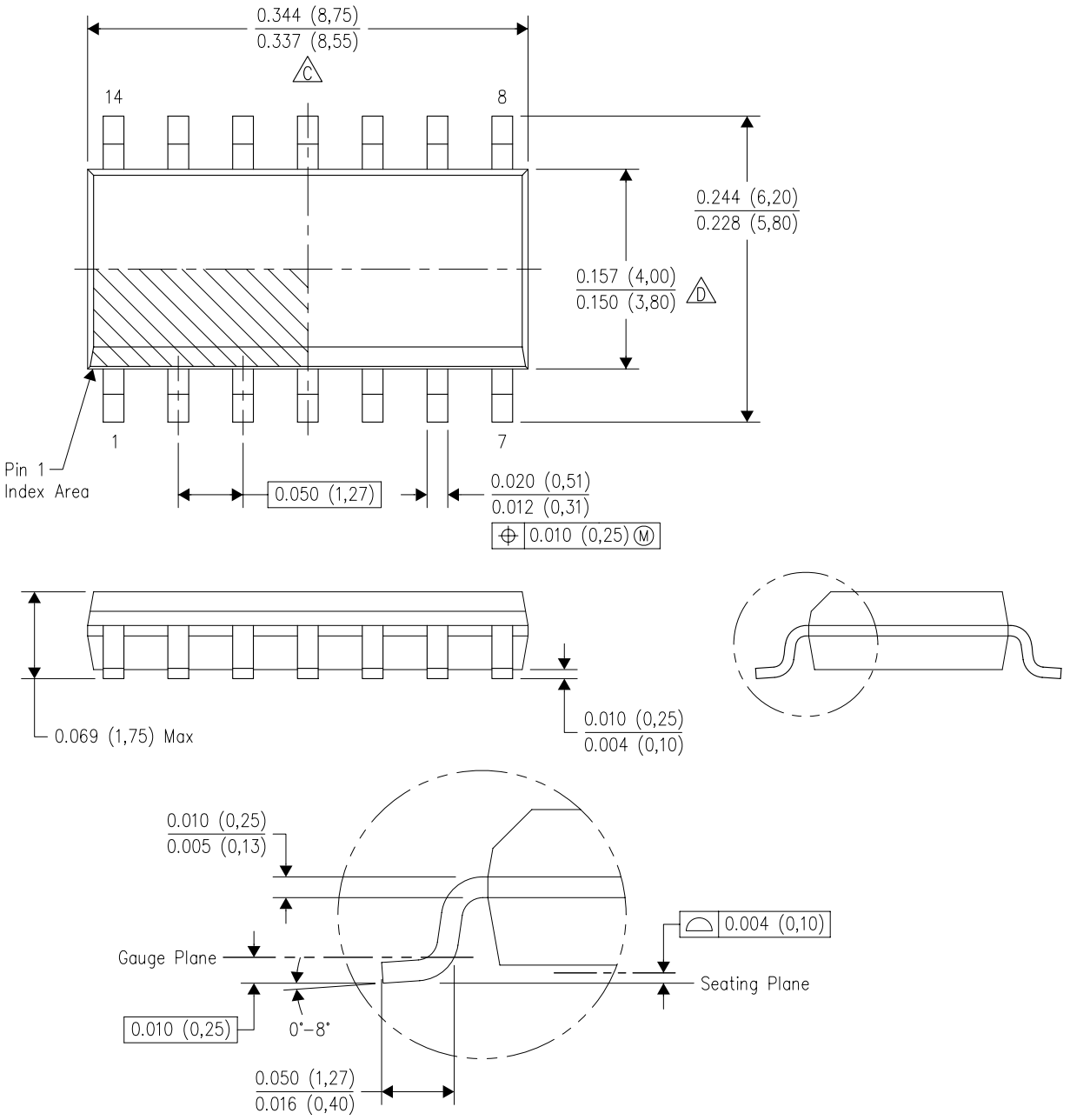
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

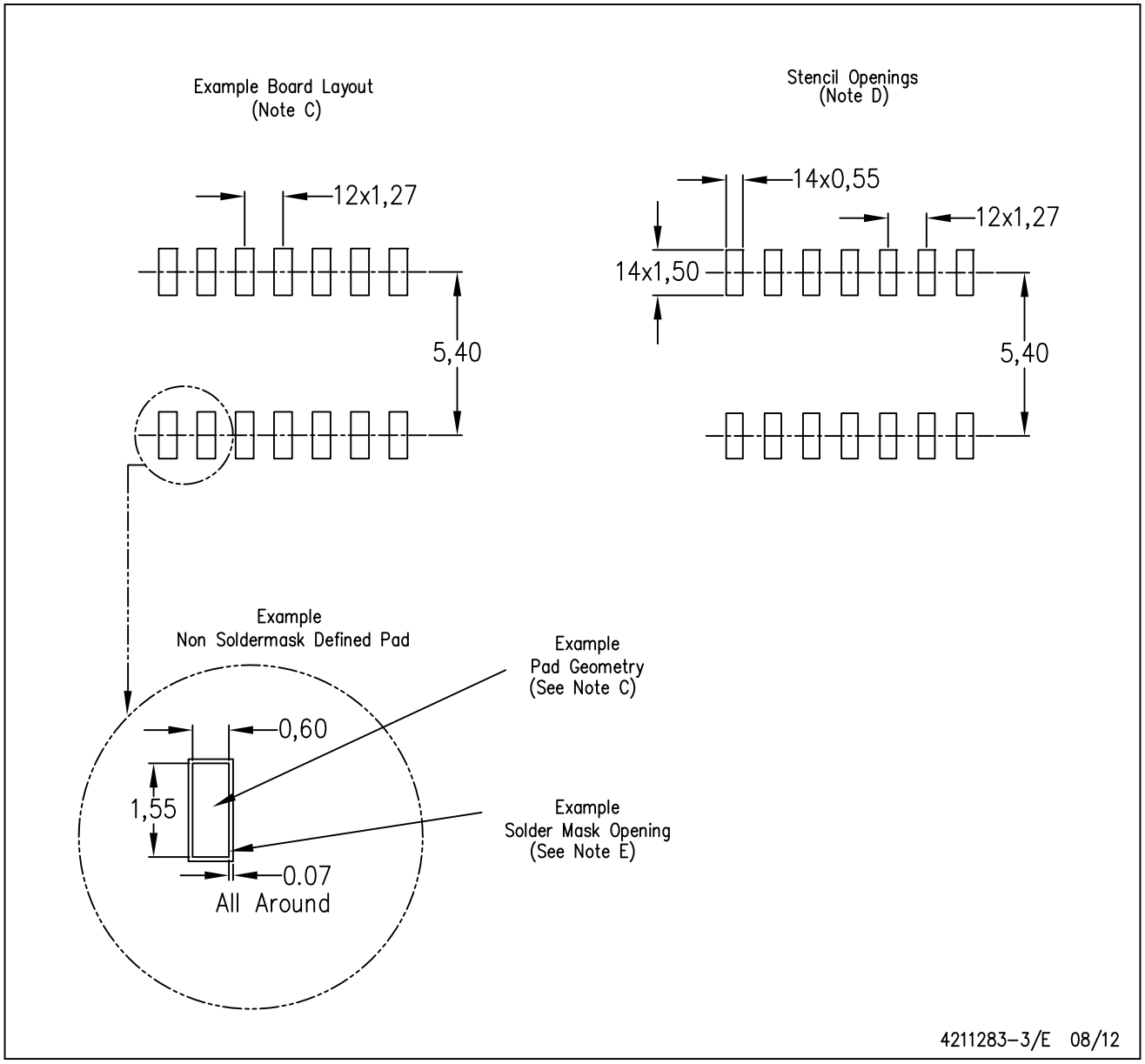
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

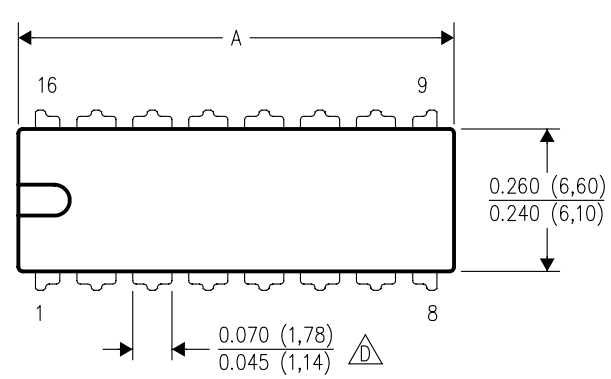


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

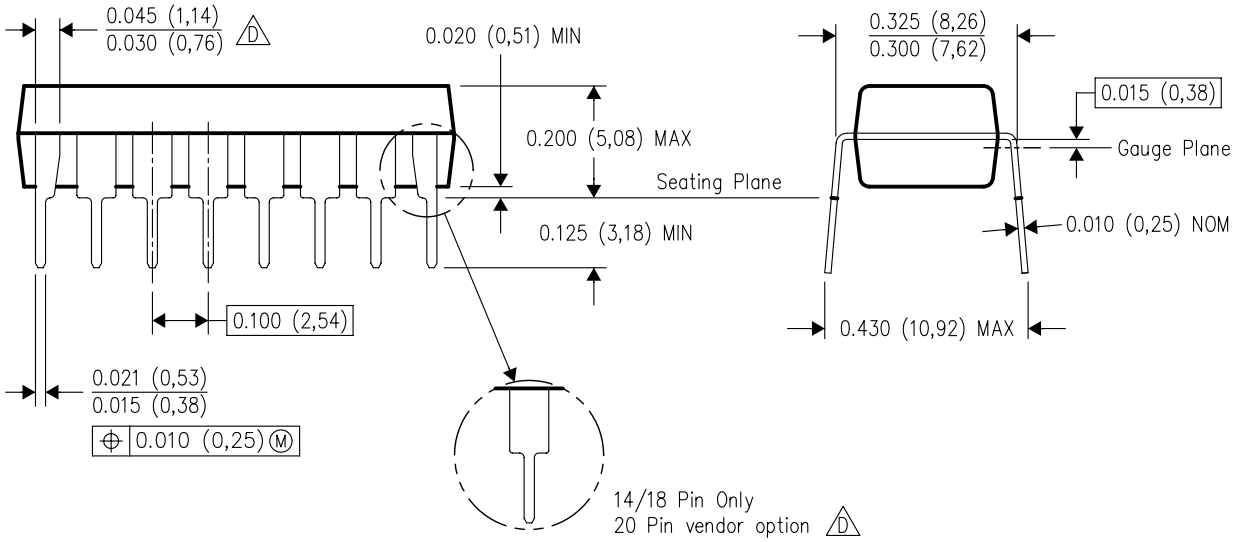
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



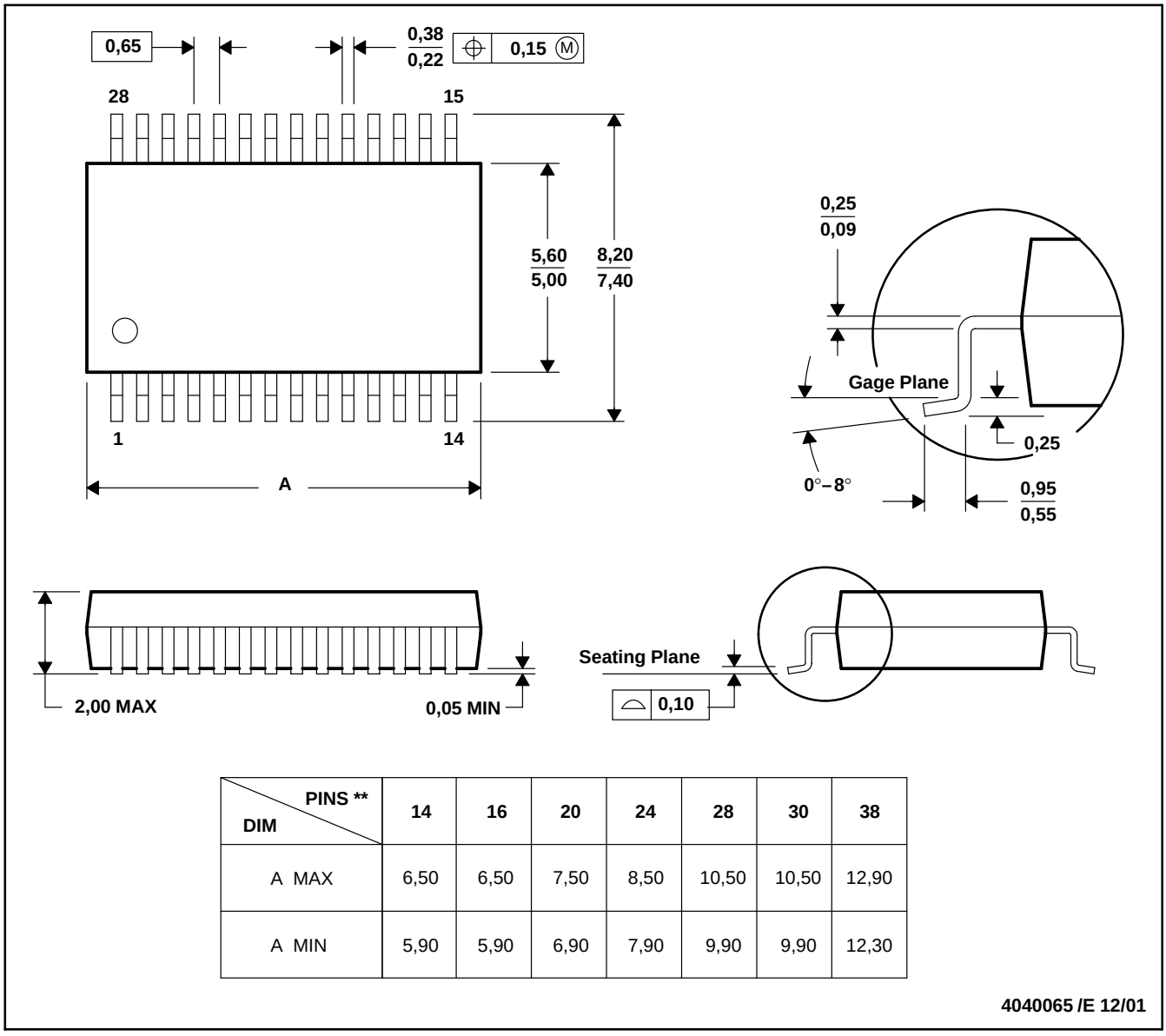
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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